

PHY IP for PCI Express 5.0



Highlights

- Supports the latest features of PCIe® 5.0, 4.0, 3.1, 2.1, 1.1, and PIPE specifications
- x1, x2, x4, x8, x16 lane configurations with bifurcation
- Multi-tap adaptive and programmable Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalization (DFE) supporting more than 36dB channel loss
- Adaptive receiver equalizer with programmable settings
- Supports lane margining at the receiver
- Supports L1 substate power management
- Power gating and power island
- Embedded bit error rate tester (BERT) and internal eye monitor
- Built-in Self Test vectors, pseudo random bit sequencer (PRBS) generation and checker
- IEEE 1149.6 AC JTAG Boundary Scan
- Supports -40°C to 125°C junction temperatures
- Supports flip-chip packaging

Target Applications

- Desktops, workstations, servers
- Automotive
- Embedded systems and set-top boxes
- Network switches and routers
- Enterprise computing and storage networks

Technology

- Available in leading processes through 7-nm FinFET

Overview

The multi-channel DesignWare® PHY IP for PCI Express® 5.0 includes Synopsys' high-speed, high-performance transceiver to meet today's applications' demands for higher bandwidth. The PHY's cost-effective solution meets the needs of today's high-speed chip-to-chip, board-to-board, and backplane interfaces while being extremely low in power and area.

Using leading-edge design, analysis, simulation, and measurement techniques, Synopsys delivers exceptional signal integrity and jitter performance that exceeds the PCI Express standard's electrical specifications. The high-margin, robust PHY architecture tolerates process, voltage and temperature (PVT) manufacturing variations and is implemented with standard CMOS digital process technologies.

The multi-tap transmitter and receiver equalizers, along with the advanced built-in diagnostics and ATE test vectors, enable customers to control, monitor and test for signal integrity without the need for expensive test equipment. This provides on-chip visibility into actual link and channel performance to quickly improve signal integrity. This capability reduces both product development cycles and the need for costly field support.

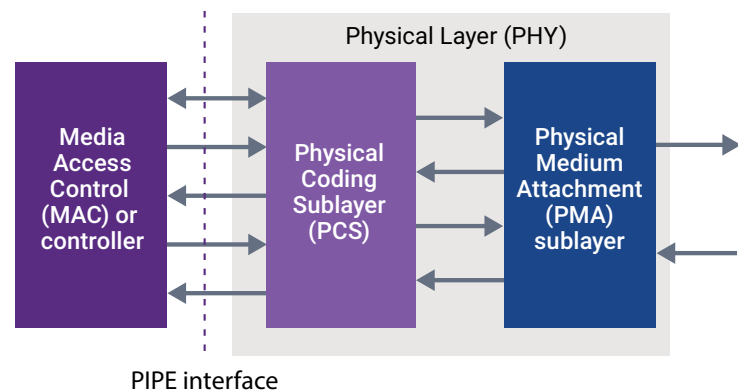


Figure 1: PCIe PHY connection to the protocol stack

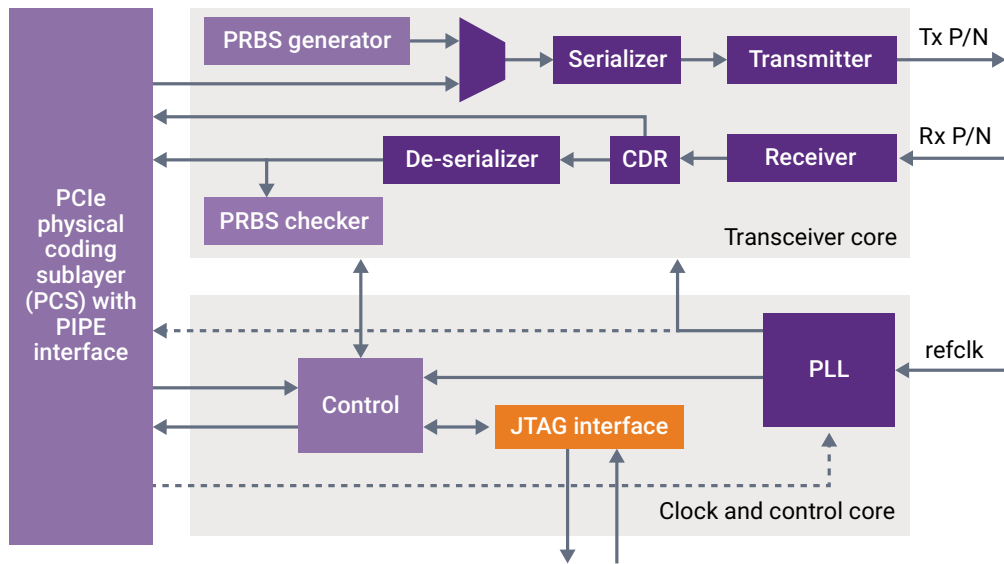


Figure 2: Single channel PCIe PHY block diagram

Key Features

- Physical Coding Sublayer (PCS) block with PIPE interface
- Supports PCIe 5.0, 4.0, 3.1, 2.1, 1.1 encoding, backchannel initialization
- Lane margining at the receiver
- Spread-spectrum clocking (SSC)
- PCIe power management features, including L1 substate; power gating and power island; DFE bypass option and voltage mode TX with under drive supply options
- The multi-channel PHY macro with single clock and control core for higher density with support for both internal and external reference clock inputs
- PIPE bifurcation as well as PHY macro aggregation for up to 16-lane configurations
- Superior Rx jitter & cross talk tolerance reduces design constraints for a wider range of board layout designs
- Automated Test Equipment (ATE) test vectors for complete at-speed production testing
- Each PHY channel contains its own 7-, 9-, 11-, 15-, 16-, 23-, and 31-bit pseudo random bit sequencer (PRBS) for internal and external loopbacks
- Each channel is fully controllable via the integrated logic core as well as the test access port (TAP)

Deliverables

- Verilog models
- Liberty timing views (.lib)
- LEF abstracts (.lef)
- CDL netlist (.cdl)
- GDSII
- ATPG models IBIS-AMI models
- Documentation

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes [logic libraries](#), [embedded memories](#), [embedded test](#), [analog IP](#), [wired and wireless interface IP](#), [security IP](#), [embedded processors](#), and [subsystems](#). To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' [IP Accelerated initiative](#) offers [IP prototyping kits](#), IP software development kits, and [IP subsystems](#). Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.