Overview

The Synopsys DesignWare® HBM2/HBM2E PHY is a complete physical layer IP interface (PHY) solution for high-performance computing (HPC), graphics, and networking ASIC, ASSP, and system-on-chip (SoC) applications requiring high-bandwidth HBM2/HBM2E SDRAM interfaces operating at up to 3200 Mbps. The DesignWare HBM2/HBM2E PHY is ideal for systems with low to modest memory capacity that require higher bandwidth than is attainable with practical DDR4-based systems.

The DesignWare HBM2/HBM2E PHY is provided as a set of hard macrocells delivered as GDSII. These hard macrocells include integrated application-specific HBM2/HBM2E I/Os required for HBM2/HBM2E signaling. The design is optimized for high performance, low latency, low area, low power, and ease of integration. The hard macrocells are easily assembled into a complete 1024-bit HBM2/HBM2E PHY. The RTL-based PHY Utility Block (PUB) supports the GDSII-based PHY components and includes the PHY training circuitry, configurations registers and BIST control. The HBM2/HBM2E PHY includes a DFI 4.0-compatible interface to the memory controller, supporting 1:1 and 1:2 clock ratios. The design is compatible with both metal-insulator-metal (MIM) and non-MIM power decoupling strategies.

Figure 1: DesignWare HBM2/HBM2E PHY block diagram

Highlights

- Supports 2.5D-based JEDEC standard HBM2/HBM2E SDRAMs with data rates up to 3200 Mbps
- 8 independent memory channels (e.g., 1024 bits)
- Pseudo-channel operation supported to enable up to 16 channels with 1024 bit PHY
- Supports up to 4 trained frequencies with <5us switching time
- DFI 4.0-compatible controller interface
- PHY independent training capability
- Comprehensive set of design-for-test (DFT) features

Target Applications

- High-performance computing
- Graphics
- Networking
- Artificial intelligence
- Machine learning

Technology

- 16-nm and below
Key Features

- Low latency, small area, low power
- Compatible with JEDEC standard HBM2/HBM2E SDRAMs
- Data rates up to 2400 Mbps for HBM2 and 3200 Mbps for HBM2E
- 4H and 8H HBM2/HBM2E SDRAM stacks supported
- Support for fast switching between 4 frequencies
- Product subcomponents designed to precisely control timing critical delay and skews
- Controller DFI-compatible interface (DFI v4.0 Addendum 2)
  - PHY supports 1:1 and 1:2 modes (PHY:SDRAM clock ratios)
- Includes 1 phase-locked loop (PLL) per PHY and digital delay lines necessary to meet timing specifications
  - PLL allows bypass mode that enables PHY to be run at low speeds
- Separate transmit DQ and transmit DQS as well as transmit Row/Col and transmit CK delay lines
  - Allows de-skew of transmit DQS/CK vs. transmit DQ/Row-Col, respectively
- Includes separate receive DQS delay lines for both rising and falling edge of DQS
- Supports 8-channel HBM2/HBM2E DRAM systems
- Supports pseudo-channels as defined in the JEDEC HBM2/HBM2E standard
- Boot time impedance calibration
- Programmable I/O drive strength matching the HBM SDRAM
- Delay line VT compensation
- Time axis data eye training
  - Internal finite state machine (FSM) allows automated training to optimum setting
  - Alternative software hooks included to allow external software to program optimum setting
- PHY VREF can either be supplied externally through a bump or use an internal VREF generator that can provide a programmable VREF for use internal to the PHY
  - Internal VREF generator is programmable from 0 to VDDQ
- Physical implementation of the top-level HBM PHY hard macro is designed to be compatible with a face centered rectangular (FCR) micro bump pattern similar to the JEDEC standard HBM2 SDRAM micro bump pattern with a minimum of 55um center-to-center spacing
  - Permits shortest 2.5D routes between PHY and HBM2/HBM2E SDRAMs for highest signal integrity
- Enhanced power savings support that includes:
  - Per-channel DFI_LP
  - PHY leakage mode with fast exit (<5us)
  - PHY controls to support DRAM retention mode
- ARM® AMBA® APB interface for configuration register access
- Test data register (TDR) interface for configuration register access
- Multiple test modes
  - Delay line oscillator test mode
  - Mux-scan ATPG
- At-speed loopback testing on both the address and data channels

Pre-hardened HBM PHYs are available in select process technologies

- Services available for custom PHY hardening requirements
- 2.5D Interposer reference designs available
Deliverables

- Executable .run installation file, including GDSII, LEF Files, LVS netlists, .lib/.db timing models, Verilog model, DRC/LVS log files, I/O IBIS model, I/O HSPICE netlist, parameterized Verilog top-level PHY netlist files, sample verification environment, PHY data book, physical implementation guide, application notes, verification guide, installation guide, implementation checklist
- The PHY Utility Block includes Verilog code, synthesis/STA constraints and scripts, sample verification environment, data book

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About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys’ IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys’ extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.