

StarRC Custom Rapid3D Extraction

Next Generation High Performance 3D Fast Field Solver

June 2010



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Executive Summary

Accurate parasitic extraction is critical to the success of today's system-on-chip (SoC) designs because of the growing use of sensitive custom circuits and the vulnerability of layout to increased process variation and parasitic effects. The nanometer SoC designers need a highly accurate three-dimensional (3D) field solver to extract larger proportions of the designs to ensure silicon success. A high-performance and high capacity field solver that is integrated with their existing post-layout extraction and simulation flow will enable designers to achieve their accuracy criteria with confidence as well as successfully meet their tight tape-out schedules. The next-generation Rapid3D technology in StarRC Custom provides an integrated 3D extraction solution to address these growing accuracy, performance, capacity and ease-of-use needs. This paper presents the new Rapid3D technology and the benefits it provides for a range of target applications, including IP characterization as well as custom analog/mixed-signal (AMS), high-speed digital and memory array designs.

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Introduction

The convergence of applications in consumer products, requiring wireless operation for mobility, is leading to an increase in the mix of digital and analog design – producing a larger use of custom circuits in today's SoC designs. In addition, the sensitivity of circuits to parasitics is intensifying at each new generation of process technology. The use of new device structures and an increasing number of metal layers introduce many new parameters that must be taken into account for accurate analysis. Technology advances elevate device and interconnect parasitics, previously considered secondary factors in older technologies, to primary factors affecting circuit behavior. For example, context-specific device parasitics—gate-to-contact coupling capacitance and gate-to-diffusion coupling capacitance—now have a profound effect on capacitance accuracy at smaller geometries. Consequently, the SoC designers are looking for 3D field solver extraction accuracy on more blocks that are larger in size and that were traditionally verified with full-chip, pattern-matching extraction solutions. In order to meet their design cycle deadlines, they need a solution that is not only highly accurate but also provides full-chip performance, capacity and ease-of-use of integration with their existing flow. This requires a fast 3D field solver that is tightly integrated into their standard extraction solution and consists of advanced process modeling and efficient data processing technologies to support increased modeling requirements and flow complexity (such as metal fill and pre-characterized cells), as well as designs containing hundreds of thousands of nets.

The next generation Rapid3D fast field solver technology, built on the gold standard Raphael™ NXT engine, is fully integrated into StarRC Custom to address the designers' growing accuracy and performance needs (Figure 1). It incorporates the latest advancements in 3D extraction algorithms to deliver an order of magnitude of speed improvement and ultra low memory usage compared to previous generation field solvers.

Rapid3D's advanced engine accounts for all 3D effects associated with the complex geometries of interconnect and device structures at smaller geometries to deliver attofarad (10^{-18} farad) accurate extraction that tightly correlates with Synopsys' Raphael, the reference field solver used by the major foundries. In addition, the integration of Rapid3D technology into StarRC Custom provides native support for the latest parasitic effects. Overall, Rapid3D's high-performance and silicon-accurate extraction, coupled with StarRC Custom's efficient process modeling and data processing technology, provides SoC designers a full-chip solution with desired field solver accuracy. The seamless integration of Rapid3D in StarRC Custom requires no additional setup, thus enabling designers to be up and running with the fast field solver extraction in a matter of minutes.

Due to its high accuracy, performance and capacity, Rapid3D technology is the ideal solution for the following timing-sensitive transistor-level applications:

- ▶ Custom AMS circuits: Rapid3D delivers sub-femtofarad resolution required for AMS designs, such as analog-to-digital converters (ADCs) and differential amplifiers, which are highly sensitive to layout parasitics.
- ▶ Ultra high performance gate-level and transistor-level digital designs: Rapid3D enables detailed analysis of high speed blocks, such as 1-GHz processor cores and datapaths, and critical nets, such as clock networks.
- ▶ Memory array designs at 45 nm and below: Rapid3D provides silicon-accurate extraction of critical bit lines and word lines to enable accurate analysis of the impact on read and write access times.
- ▶ Library and IP development starting at 45 nm: Rapid3D's fast runtime and low memory usage enables efficient full cell and library characterization.

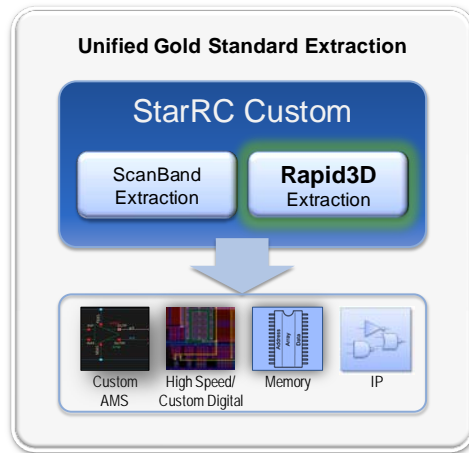


Figure 1: The embedded Rapid3D technology in StarRC Custom offers high-performance 3D fast field solver extraction for next-generation custom designs.

The following sections describe the highlights and the benefits of Rapid3D technology in detail.

Rapid3D High Performance and Capacity

Building on the Raphael NXT engine, the brand new Rapid3D extraction consists of advanced random walk technology that delivers up to 20 times faster 3D extraction versus the traditional random walk solvers and 6 times more capacity. Rapid3D's advanced random walk technology solves the electrostatic equations in 3D and computes capacitances between any pair of nets in a layout with unmatched performance while maintaining the gold standard accuracy. The random walk method is a production proven technique for extracting layout parasitic capacitances and has been used for highly accurate extraction by leading foundries and design companies for over a decade. Unlike other field-solver technologies, random walk solvers allow users to specify accuracy bounds and it then delivers repeatable results consistent with the user specified accuracy.

Rapid3D significantly improves on the traditional random walk technology by incorporating the latest advancements in field solver algorithms that not only deliver higher performance but also higher accuracy compared to the alternate field-solver technologies such as the Finite Element Method (FEM) and the Boundary Element Method (BEM) or any advanced variation of such traditional technologies. In addition, Rapid3D shares the ultra fast geometry processing technology of StarRC's ScanBand engine, enabling efficient processing of very large designs.

As a result of the latest advancements in Rapid3D, SoC designers can extract capacitances of nets in a large block or the entire chip in considerably less time. Rapid3D only stores the conductor geometries and dielectric distribution within a layout region in memory, rather than the mesh of points in the entire layout region. Such memory limited architecture is inherent advantage of Rapid3D technology over solvers based on FEM or BEM methods. In addition, the memory usage is completely independent of the desired accuracy level.

Figure 2 shows the performance and memory usage of Rapid3D for over 50 customer designs, ranging across various process nodes, compared to traditional field solver solutions.

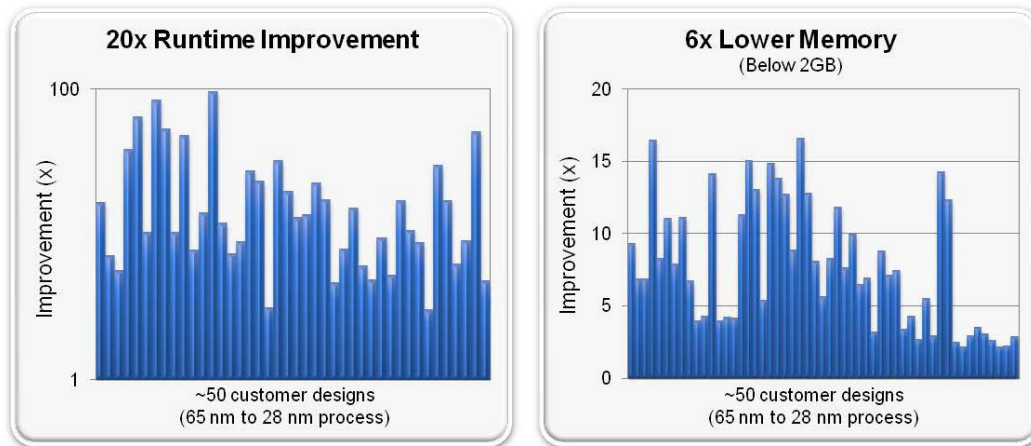


Figure 2: Rapid3D delivers 20x runtime improvement and 6x lower memory.

Highly Linear Multicore Scalability

In addition to the considerable speedup that Rapid3D natively provides on a single core, it also delivers highly linear performance scalability with its advanced multicore technology. A highly scalable distributed processing capability allows designers to achieve high throughput and maximize the use of the multicore hardware by distributing the jobs across available cores, within a single server or multiple servers on a compute farm. As shown in Figure 3, Rapid3D’s multicore technology has demonstrated up to 54 times speed improvement on 64 cores on customer designs.

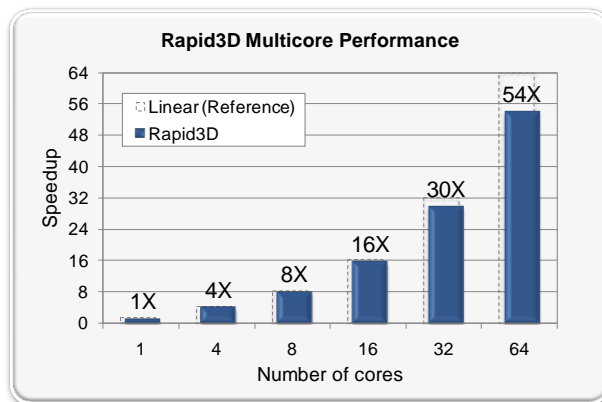


Figure 3: Rapid3D provides highly linear performance scalability using multicore technology.

Rapid3D also incorporates efficient multithreading that allows you to distribute a given job over several cores within a box. The multicore threading can be used in a highly optimized scheme alongside multiprocessing to enable the optimal use of the resources in a memory-constrained environment.

If a core becomes unavailable, Rapid3D multicore technology includes a built-in fault tolerance capability that allows the processing to proceed without interruption by transferring the processing to another available core. Additionally, Rapid3D

offers smart load balancing that utilizes waiting cores on the fly to slice the long pole jobs and prevent any degradation in the turn-around time.

Rapid3D's inherent performance, along with its multi-core capability, enables designers to accurately extract and analyze large blocks consisting of hundreds of thousands of nets or more. Table 1 shows Rapid3D's performance scalability on a 64 x 32 MB memory array block with varying numbers of cores at an accuracy setting of 0.5 percent. The data shows that Rapid3D extraction completes on one core in a single working day. Also, the extraction completes in only 35 minutes when using 16 cores—a tremendous speedup of 15 times. In addition, a key advantage of the Rapid3D technology is the low peak memory usage that remains constant regardless of the number of cores used. Typically, given the ultra-low memory usage, one can run full-chip designs using Rapid3D on a machine with two GB of memory per core.

	1 Core	4 Cores	8 Cores	16 Cores
Runtime (minutes)	503.9	126.6	64.4	34.6
Speedup	1.0	4.0	7.8	14.6
Peak Memory (MB)	794	794	794	794

Table 1: Rapid3D demonstrates highly linear scalability on a memory array design with a 0.5 percent accuracy setting.

Another important application of Rapid3D technology is the characterization of critical analog blocks and standard cell libraries for full-chip simulation. Since the standard cells serve as building blocks for the full-chip design and are characterized only once, designers look for the highest accuracy to meet the stringent timing constraints and accurate silicon correlation. Rapid3D enables designers to characterize circuits to their desired accuracy and provides the ability to characterize an entire standard cell library overnight. Table 2 shows the runtime for a representative subset of standard cells in a 32-nm library using Rapid3D on four cores. A typical standard cell can be characterized in under 2 minutes.

32-nm Cell	Rapid3D Runtime on Four Cores (seconds)
INV	36
AND2	50
NOR3	62
MUX4	76
NOR4	85

Table 2: Rapid3D extracts typical 32 nm library cells under 2 minutes with a 0.5 percent accuracy setting.

The high accuracy, performance and capacity of Rapid3D, combined with its highly scalable multicore technology, provides designers with a full spectrum of options to meet the needs of their target applications ranging from library characterization to full-custom design extraction.

Flexible Accuracy Continuum

Rapid3D extraction correlates tightly with silicon, as shown in Figure 4.

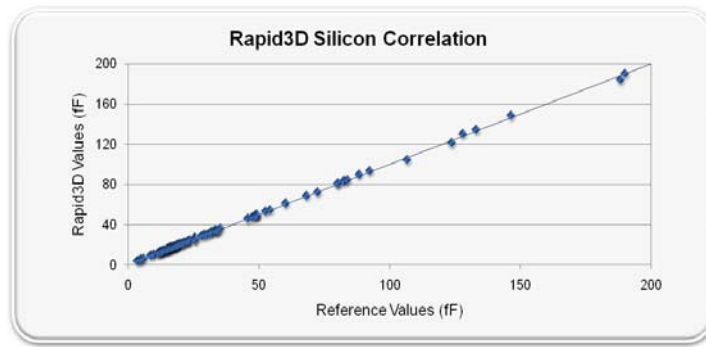


Figure 2: Rapid3D closely correlates with silicon.

Besides its gold standard attofarad accuracy, another key advantage of Rapid3D technology is that it provides a continuum of accuracy tuning for various extraction needs. Rapid3D enables designers to customize the extraction to the specific accuracy requirements of the circuit, thereby providing a flexible tradeoff with performance. This flexible accuracy and performance tradeoff is a distinct advantage of the Rapid3D random walk technology compared to FEM or BEM based field solvers, which do not offer similar benefits. It allows designers to better control the accuracy and avoid setting pessimistic margins during analysis that could lead to overdesign or underdesign.

Different design applications, as well as specific nets, might have different accuracy requirements because of the sensitivity of the circuit of interest to parasitics. For example, a typical gate-level extraction job might require an accuracy level of five percent, while the characterization of standard cells or critical analog circuits might require an accuracy level of one percent. Figure 5 shows the runtime and memory usage for extracting a set of nets at different accuracy levels ranging from one to five percent using Rapid3D. The runtime drops sharply as the accuracy goal is relaxed, while the memory usage remains constant at 155 MB.

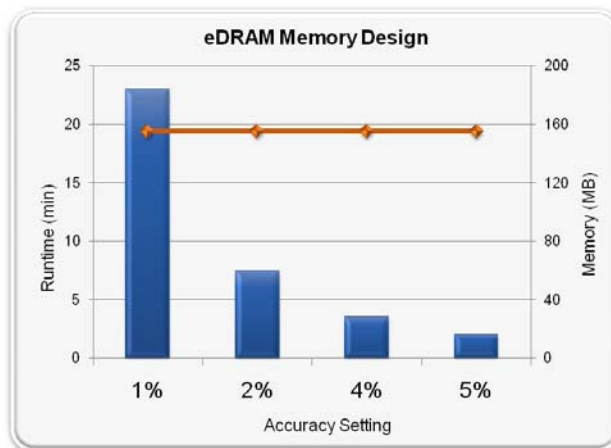


Figure 5: Rapid3D extraction accuracy can be tuned to target application needs.

StarRC Custom Integration

Historically, field solvers were used in initial design stages to characterize a process or in special scenarios that required high accuracy to characterize a critical block or cell. Designers used field-solver-type extractors, which required time-consuming setups and difficult integration into post-layout flows, outside of their signoff flow, for validation or extraction. The situation is exacerbated in smaller geometries due to the new parasitic effects that require advanced process modeling to achieve good correlation with silicon, as well as high yield. For example, with the transition to 32 nm, modeling the via and contact size changes and double-patterning lithography to achieve the dimensions for printed

circuits are crucial for silicon correlation. The setup time required to accurately model the numerous process effects and create input data for field solver extraction introduces a significant overhead that is impractical given the growing design sizes and ever-increasing project cycle-time constraints. The Rapid3D field solver flow takes full advantage of the industry leading process modeling technology of StarRC Custom and its widely qualified and used process modeling interface, the Interconnect Technology Format (ITF), to accelerate the extraction flow.

Additionally, as design complexities increase, designers are looking for a push-button field solver solution that can handle the capacity of full-chip flows while providing field-solver accuracy on critical blocks and nets. Designers require complementary solutions involving pattern matching and field solver extraction techniques to provide them with the complete flexibility of accuracy and runtime in their post-layout verification flows, without the overhead of supporting and qualifying multiple tools and input files. Rapid3D integration into StarRC Custom enables designers to use its existing signoff flow consisting of standard inputs and familiar user interface for increased efficiency. It provides designers access to field-solver accuracy through a single StarRC Custom command file option and requires no additional setup for integration into their sign-off design flows for post-layout analysis. This means the inputs (command file) and outputs (parasitic netlist for simulation) of the extraction flow remain exactly the same as existing StarRC Custom flows, and designers can be up and running with a field solver for various applications in a matter of minutes. Figure 6 below shows the integration of the Rapid3D technology within the StarRC Custom framework.

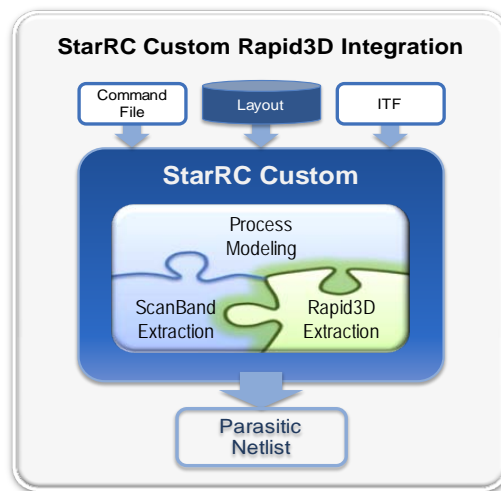


Figure 6: Rapid3D integration with StarRC Custom delivers proven reliability, modeling, and ease-of-use.

Rapid3D fast field solver extraction is invoked internally through the same StarRC Custom command file and supports all StarRC Custom options automatically. The integrated solution offers a seamless interface with all standard input design formats, including GDSII interface for custom design flows and Milkyway or LEF/DEF interfaces for gate-level automatic place-and-route (APR) design flows. The output of the Rapid3D field solver extraction plugs directly into standard output netlist formats including DSPF, SPEF, and SBPF (Synopsys Binary Parasitic Format) to interface with downstream analysis and simulation tools. The solution supports all advanced flow-specific features such as flexible ignoring of device parasitics (those included in SPICE models), hierarchical skip_cells feature for pre-characterized blocks and metal-fill extraction, which are common in today's design flows. Commonly used and well-known features and commands available in StarRC Custom are automatically supported in Rapid3D field solver extraction by simply setting a single option to invoke the field solver technology, thus providing user-controlled flexibility for accuracy.

The integrated StarRC Custom and Rapid3D solution has two different operating modes:

- ▶ FSCOMPARE mode: Compares the extracted value from StarRC Custom and the Rapid3D field solver.
- ▶ FS_EXTRACT_NETS mode: Performs complementary high accuracy extraction of critical circuits.

Within the StarRC Custom environment, designers can supply Rapid3D with a list of nets that require the highest level of capacitance extraction accuracy instead of all net extraction. StarRC Custom intelligently partitions the polygons in the design, applies Rapid3D technology on subset of the design and produces a single netlist for all nets with field-solver accurate results on user specified nets. The netlist can then be easily plugged into a simulation environment for circuit

analysis. This flexibility of full-chip capacity with field-solver accuracy provides a complete spectrum of extraction technologies within a single extraction flow to boost designer productivity.

Conclusion

Field solver extraction with full-chip performance and capacity is required to meet the growing accuracy demands of SoC custom designs. The next generation embedded Rapid3D technology in StarRC Custom offers up to 20 times speedup in single-core performance compared to traditional field solvers, ultra-low memory usage and attofarad accuracy. Rapid3D's highly scalable multicore technology offers up to 54 times performance boost on 64 cores, thereby enabling designers to extract larger designs with performance and capacity comparable to full-chip signoff extraction solutions. The integration of Rapid3D in StarRC Custom delivers proven reliability, modeling and ease-of-use, allowing designers to easily access the technology within their existing design flows with no additional setup and using standard interfaces that significantly accelerates the overall turn-around time.



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