StarRC™ Custom: Next-Generation Modeling and Extraction Solution for Custom IC Designs

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Executive Summary

IC design is facing significant challenges beyond the 40-nm process technology node because of increased process variation and its impact on circuit behavior and performance. At advanced process nodes, the increasing number of layers and new device structures result in hundreds of new parameters and many new parasitic effects, which require higher levels of accuracy in modeling and parasitic extraction for simulation and signoff analysis. Custom digital, analog/mixed-signal, and memory designs are particularly sensitive to the nanometer device parameters and parasitics. At 40-nm process technology and beyond, approximating or ignoring the new interconnect and device effects in custom designs can lead to inaccurate post-layout simulation results and jeopardize the chances of successful silicon. The Synopsys StarRC™ Custom extraction solution offers a wide range of features including advanced interconnect and device parasitic modeling and extraction that enable increased signoff accuracy and productivity for today's system-on-chip (SoC) custom IC designs.

Introduction

The convergence of consumer, wireless, mobile, and computer applications is leading to the merging of digital and analog circuits in today's advanced SoC designs, resulting in a proliferation of custom IP in these designs. The custom IP, such as custom digital, analog/mixed-signal, RF, or memory circuits, have stringent performance, signal integrity, and power requirements in order to meet demanding SoC design objectives. These circuits are also highly sensitive to physical effects, including the new device and interconnect parasitic effects of the advanced process geometries. Thus, the accuracy of the device and interconnect models, as well as that of the extraction and post-layout verification tools, is paramount to ensuring the desired behavior and performance of custom circuits and SoC designs.

The key challenges faced by custom circuit designers at the device-level are associated with:

▸ Context-specific device parasitics
▸ Designed resistors
▸ Advanced MOS device parameters
▸ Power networks with multiple substrate contacts
▸ Analog symmetric nets

Context-Specific Device Parasitics

Custom IP designers use foundry-provided SPICE models for circuit simulation. These SPICE models characterize multiple parasitic effects such as MOS gate-to-contact capacitance, MOS gate-to-source/drain capacitance, source/drain capacitance, resistor-body-to-bulk capacitance, and capacitor-plate-to-bulk capacitance. The SPICE models are typically developed from test chips where the devices may be placed in isolation for behavioral analysis. However, in a real design, many of these devices are placed in close proximity to each other, resulting in increased parasitic interaction. As more circuits are compressed together in advanced process technologies, the parasitics become context-specific or layout-dependent. The increased interaction between interconnect and device layer polygons brings significant changes at the device level, requiring higher accuracy in device and interconnect parasitic extraction.

In particular, custom circuits are very sensitive to gate-to-contact capacitances and contact resistance. Previously, gate-to-contact capacitance was included in SPICE models. These SPICE models were derived by measuring MOS IV (current vs voltage) characteristics with specific contact placements to the gate terminal of the device. However, at advanced nanometer process nodes, these specific placements to the gate node do not yield accurate SPICE models for post-layout simulation as the gate-to-contact distance and interaction can vary significantly in actual layout. Thus, custom designers now generally use one set of SPICE models with gate-to-contact capacitance for pre-layout simulation and another set of SPICE models without gate-to-contact capacitance for post-layout simulation, but instead using extraction tools to extract the capacitance for post-layout. In addition to contact capacitance, contact resistance also plays an important role in device response. In advanced process technologies, the diffusion contact resistance is much larger than the metal interconnect resistance. Hence, accurately extracting gate-to-contact coupling capacitance and diffusion contact resistance on power nets is imperative for 40-nm custom designs.

Designed Resistors

Designed resistors are an integral part of all custom circuits. For instance, designed resistors are used in differential amplifiers, differentiators, ADCs, and DACs. These resistors are formed with poly, diffusion or metal, depending upon the precision and resistance value needed. The body of designed resistors contributes significant capacitance, which needs to be taken into account for post-layout simulation. The designed resistors placed next to each other can have significant noise impact on simulation accuracy.

Advanced MOS Device Parameters

Transistor-level custom designs are also highly sensitive to advanced device properties like source/drain capacitance, stress parameters, the number of contacts, and well-proximity effects. An extraction tool needs to handle these with extreme care and ensure that device properties are associated with the correct terminals; not doing so would lead to inaccurate simulation results and compromise success.

Power Networks with Multiple Substrate Contacts

The performance of a custom IP is very sensitive to voltage drop on the power line and back-bias voltage on the MOS device. To ensure that each device in a well has minimal back-bias voltage, designers add multiple substrate or well taps on the power line in the layout. Extraction tools often consider bulk layers of the device to be ideal. Hence, when multiple taps are added on the power line in a given well, part of the power net parasitics may be shorted out because of the ideal bulk-layer connection to the power net. It is important that multiple taps in a well do not short the parasitics to ensure proper timing simulation with power net parasitics.

Analog Symmetric Nets

One basic characteristic of custom analog circuits is the use of differential signals to improve the performance and gain, as shown in the example in Figure 1. The behavior of the circuit is impeded if these differential signals are not symmetric. Since these circuits are very sensitive to parasitics, designers take extreme care to ensure that the environment and process variation of each differential signal are identical. This improves the manufacturing yield. As a result, custom designers expect the same resistance and capacitance values for both signals in a differential pair. When an extraction tool reports different capacitance values for differential nets, custom designers analyze the layout in great depth to find the asymmetry.
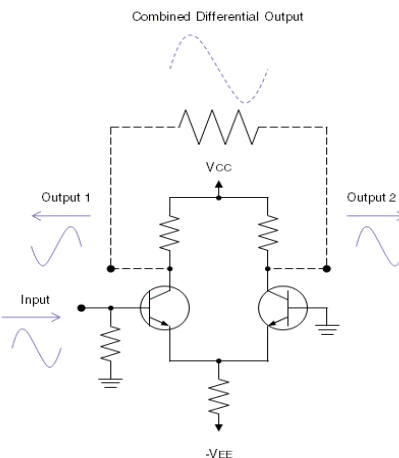

Figure 1: Accurate and consistent parasitic extraction is required for sensitive analog symmetric nets such as in a differential amplifier.

In the case of memory designs such as SRAMs, designers are concerned about the parasitics in the word lines and bit lines. In SRAMs, designers use bit-line pairs (BIT and BIT-bar) to read and write data. To improve the memory read time, a sense amplifier detects a small differential voltage change on a bit-line pair. Hence, it is very important to extract symmetric net capacitances on bit-line pairs.

StarRC™ Custom Advanced Parasitic Extraction Solution

StarRC Custom is the advanced parasitic extraction solution for next-generation custom digital and analog/mixed-signal (AMS) IC designs. A key component of the Synopsys Galaxy™ Implementation Platform, it is built on Synopsys' proven gold standard extraction technologies but uniquely tooled for custom design in advanced process technologies (see Figure 2). StarRC Custom offers advanced parasitic modeling and silicon-accurate extraction for high-sensitivity custom circuits. It delivers high performance with tuned accuracy to meet the stringent demands of the custom designs. This paper describes StarRC Custom's advanced capabilities and techniques to address the custom design challenges described above.
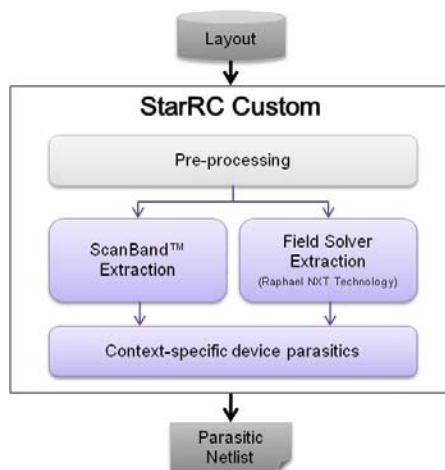

Figure 2: StarRC Custom's unified gold standard extraction technologies deliver high accuracy and performance for custom IC designs.

Handling MOS Diffusion Contacts

Diffusion contact resistance and capacitance (shown in Figure 3) play a very important role in transistor performance in deep submicron technology. Deep-submicron diffusion contacts are taller, and the spacing between the diffusion contact and gate is reduced significantly. This has a profound effect on SPICE simulation because the contact-gate capacitance acts as a Miller capacitance. As the contact comes closer to gate, the coupling capacitance has a larger effect on circuit performance. One can account for this gate-to-contact coupling capacitance by performing a complete coupling capacitance extraction in a post-layout flow. However, this would lead to a longer extraction run time and larger netlist. A larger netlist increases the post-layout simulation run time significantly. Studies show that for cell characterization, it is important to retain gate-to-contact coupling while grounding the other coupling between the nets.
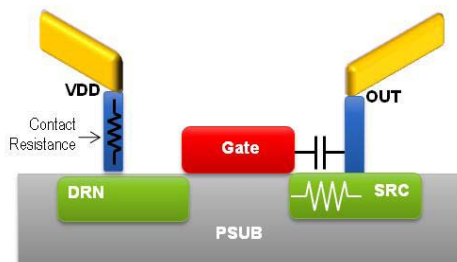

Figure 3: Contact resistance and capacitance have a profound impact on custom circuit performance and therefore must be extracted accurately.

During cell characterization, many designers extract both the power network and the signal network for post-layout simulation. This ensures that the post-layout simulation captures the voltage drop due to power-network parasitics and coupling effects between signals. However, the resistances of contacts at 65 nm and 45 nm are significantly larger than metal resistances. The contact resistance is of the order of 60 ohms, whereas the metal resistance is in the milli-ohm

range. Hence, extracting the complete power network for standard cell characterization is not very efficient as it increases the number of parasitics in the post-layout simulation netlist significantly. Extracting the contact resistance alone for the power network by treating other power metal and via layers as ideal conductors is sufficient to ensure accuracy.

StarRC Custom has the unique ability to retain gate-to-contact capacitance while grounding other coupling capacitances. StarRC Custom can also extract contact resistance on power networks while treating other layers in the power network as superconductors. This ensures a minimum loss of accuracy without sacrificing cell characterization turnaround time. One user of this flow has seen up to 8x boost in productivity with only 2% delay change.

Handling Designed Resistors in Custom Circuits

Designed resistors are used in every custom design. These resistors are drawn separately or in groups, as in a resistor bank. Resistors in a resistor bank are connected in series and parallel combinations to achieve specific resistance values. Moreover, sometimes not all resistors in a bank are used; some can be left floating or left dangling for future enhancements through metal mask changes.

As feature size and spacing reduce from node to node, closer interaction occurs between the resistor body, interconnects and resistor terminals. Figure 4 shows the capacitances of importance:

- Resistor body to bulk
- Resistor body and terminal to nearby conductor
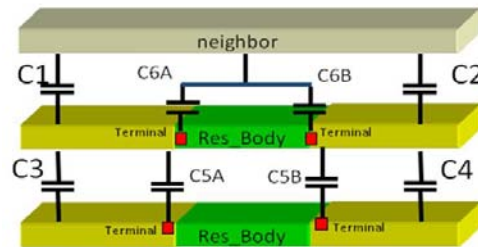- Resistor body and terminal to nearby resistor body and terminal

Figure 4:   Resistor body coupling capacitance extraction is needed to ensure post-layout simulation accuracy in advanced process technologies.

Previously, resistor models did not account for coupling effects from nearby geometries. This was reasonably accurate for old process nodes. To account for the capacitances of the resistor body and terminals, resistors were either modeled with a simple PI model with one resistor and two capacitors or a Y model with two resistors with a single capacitance from the center node. This lead to significant optimism or pessimism in simulation results as the proximity of a large resistor body contributes to significant coupling capacitance. If the adjacent resistor is not used, then the capacitance between resistor body and terminals needs to be grounded. If the adjacent resistor is connected to different net, then there should be a coupling capacitance between the terminals of the two devices to account for noise. Furthermore, when a signal line runs on top of a resistor or by the side of the resistor, then there should be a coupling capacitance between the resistor body and nearby signal needs to account for induced noise between interconnect and resistor terminals.

Our experiment with SPICE simulation has shown that simulation response improves or degrades significantly depending upon whether the resistor devices belongs to the same net or different net. In the case of a simple poly resistor bank, we have seen an approximately 50 percent degradation of the signal delay.

StarRC Custom has the unique capability to extract resistor body coupling to nearby resistor terminals or nearby interconnects and coupling to the appropriate terminals. This ensures accurate post-layout simulation results with designed resistors.

Handling UDSM Device Properties in a Cross-Reference Flow

In 65-nm and 45-nm process nodes, the number of device parameters has increased significantly. These new parameters include well-proximity effects, stress effects, the number of contacts, and the number of diffusion bends. The properties extracted by physical verification tools are passed to a netlist for post-layout simulation. However, some of these properties are associated with the device, while others are associated with the device terminals. Not associating properties with their respective MOS device terminals leads to inaccurate simulation results.

In the past, device parameters such as area of the source (AS), area of drain (AD), peripheral length of source (PS) and peripheral length of drain (PD) could be associated intuitively with the drain or source terminals. However, nowadays, the

device properties have user-defined names that might be difficult to associate with a device terminal. You could parse a LVS rule file to identify whether an extracted device property is associated with the drain or source; however, in many cases, the device property extraction commands are encrypted by foundries, making it impossible to know which layer is used to extract the device parameters.

Normally, extraction tools do not need to know whether a property is associated with drain or source of a transistor. If an extraction tool reads the netlist from the LVS tool and merges the interconnect parasitics, then the results of the SPICE simulation would be accurate. However, if you want to include schematic information in parasitic netlist, then it is important for the extraction tool to know whether a property belongs to the drain or source of a transistor. Most physical verification disregards schematic device terminals when extracting layout. Hence, this leads to the swapping of device terminals when cross referencing the schematic and layout.

Since the terminals of the MOS devices can be swapped during LVS, StarRC Custom reads special attributes from the LVS cross-reference table and user-defined information to ensure that terminal properties are associated with the correct device terminals. This leads to accurate post-layout simulation results without affecting physical verification tool setup.

Handling Well Contacts

As mentioned in the previous section, designers extract power nets along with signal nets for accurate timing simulation results. Power nets are global in nature and connect to the bulk terminals of devices. The voltage of these bulk nodes, which are wells and substrate layers, play a significant role in performance of custom designs. Hence, the placement of substrate taps and well taps has a significant effect on circuit behavior due to the back-bias effect. To ensure a proper connection to the bulk, many extraction tools treat the bulk node as ideal and connect it to global VDD or GND. This results in inaccurate circuit behavior that does not account for the back-bias effect. Some extraction tools consider a well layer to be ideal and couple it to a signal net. This coupling helps in comprehending substrate noise in a SPICE simulation. However, an ideal bulk polygon with multiple well taps shorts the power network parasitics, as shown in Figure 5. This leads to inaccurate voltage drops in reliability analyses as well as incorrect power network resistances in timing simulation.
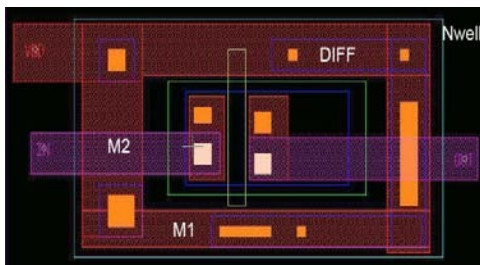

Figure 5:   Bulk shorting due to multiple taps can lead to inaccurate voltage-drop measurements.

One attempted solution has been the extraction of bulk layers along with the power network. Since there are multiple taps and multiple MOS devices in a well, you cannot do a simple tree extraction for bulk layers. Hence, this would require a mesh extraction, leading to an explosion in the post-layout netlist and a significant increase in simulation run time.

StarRC Custom addresses this challenge through a novel approach – it chooses one substrate connection or well tap in each substrate or well. This ensures that every isolated well has its own connection on the power network for an accurate voltage-drop measurement during simulation. Since only one well or substrate tap is chosen in each well or substrate, there is no shorting even if the bulk layers are treated as ideal, as shown by the data in Table 1. This also ensures that there is no increase in netlist size, providing an added advantage of simulation turnaround time.

Point-to-point resistance without well	Point-to-point resistance with ideal well	Point-to-point resistance with selected contact and ideal well
4.082 ohms	0.002 ohm	4.082 ohms

Table 1:   StarRC Custom provides a novel single tap solution for voltage-drop analysis accuracy.

Handling Symmetric Nets

In the past, geometric extractors were based on simple area and fringe capacitance equations. These tools evaluated two-layer overlaps and same-layer next-neighbor lateral spacing to compute capacitance. The advantage of this simplistic model was that it ensured consistent capacitance values for symmetric nets. Unfortunately, area and fringe capacitance models are not accurate for advanced node processes.

The geometric extractors of today, such as StarRC Custom, use pre-characterized 3-D models to extract parasitics in layout. These tools analyze multilayer interaction and the neighbor's neighbor to compute resistance and capacitance. These tools not only look at neighbors but also at the entire environment to take into account density for thickness and width variations. Since these process effects significantly influence parasitics, tools like StarRC Custom are ideally suited for advanced node processes. However, some extraction tools report asymmetric capacitance values for symmetric nets within an accuracy limit. This problem confounds analog and memory designers since it is contrary to their expectation and leads them to question the accuracy of the extraction results. The designers might also be unsure whether to modify the layout or to proceed to post-layout simulation.

StarRC Custom extracts symmetric total capacitance and coupling capacitance values for symmetric layout by controlling the examination of polygon edges, capacitance evaluation, and capacitance model lookup without loss of accuracy. Table 2 summarizes the consistency of StarRC Custom for various designs.

Design	Capacitance Range (fF)	Consistency
Digital block placed multiple times in different orientation	5.60644 - 5.66425	1.02%
Coupling capacitance between two nets in an ADC block rotated at 0 and 90 degrees	49.3376 - 49.5497	0.43%

Table 2: StarRC Custom delivers consistent extraction results for analog symmetric nets.

Conclusion

As the complexity of custom analog and mixed-signal designs continues to rise with advancing process technology, extraction tools are faced with several challenges to meet the stringent accuracy and turnaround time requirements. StarRC Custom provides advanced features to address these challenges including accurate extraction of context-specific gate-to-contact capacitance, contact-resistance, substrate taps, device properties, and symmetric nets without affecting the runtime and capacity. This allows designers to have unprecedented insight into circuit behavior during post-layout simulation and enables them to tapeout with increased confidence while meeting their design cycle times.

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