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Signoff-Driven Timing Closure ECO in the Synopsys Galaxy Platform

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Author

James Chuang
Technical Marketing Manager, Synopsys

Abstract

Increasing design complexities and the rapidly increasing number of scenarios impede the timing closure process. ECO techniques that have good single-pass fix rates can reduce the number of iterations through the extraction, implementation, and final signoff loop for fastest timing closure.

This paper explains how the timing ECO flow delivers fast, predictable, signoff-driven timing closure in a single pass. It covers a new physically-aware architecture; which runs on a single machine or across compute farms, on designs with over 100 million instances, and reduces tapeout schedules by weeks during timing closure and signoff; one of the most critical phases of IC design.

Introduction

In advanced IC designs, the need for higher performance and richer SoC features lead to increased design complexity. The advanced process technologies enable chips with higher device densities and faster speeds, but they also create new challenges for physical implementation and timing closure.

The adoption of a predictable ECO flow that eliminates violations in all signoff scenarios without inadvertently introducing new ones helps reduce the number of timing iterations required for final signoff. Static timing analysis tools provide predictable, signoff-accurate guidance to implementation tools with the following capabilities:

- Fix design rule constraint (DRC), setup, and hold violations without creating new violations (therefore preventing a “ping pong” effect).
- Perform pessimism reduction techniques such as advanced on-chip variation (AOCV), parametric on-chip variation (POCV), and path-based analysis (PBA) across all scenarios.
- Consider physical design information to achieve best quality of results (QoR) and reduce major perturbations for designs already placed and routed.

Today’s ECO guidance solutions must also be scalable to rapidly turnaround large complex designs, so design teams can quickly identify and repair numerous violations.

Timing Closure Requires Signoff-Driven Approach

Implementation tools use timing-driven algorithms for placement, clock tree synthesis, and routing. They share common timing engines with signoff timing tools to ensure close correlation between physical design and signoff timing results.

Timing violations can still arise after place and route for the following reasons:

- Implementation tools might not have constraints for all scenarios. This can lead to new violations during signoff as the signoff timer identifies violations from these new, additional scenarios.

- Design reuse continues to grow. IP design teams sometimes overconstrain selected blocks to ensure operation at higher frequencies than required for the current design. While this approach enables reuse in other chips, it can lead to different timing constraint differences between the implementation and signoff tools.

When violations appear during final signoff, design teams need a methodology that closes timing violations quickly and efficiently. Such a methodology is shown in Figure 1.

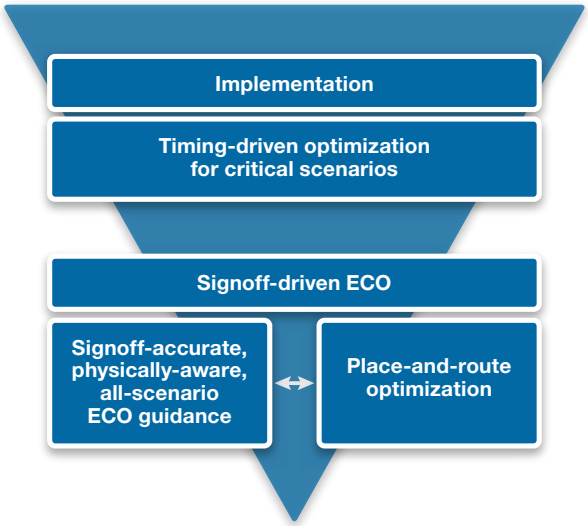


Figure 1: Signoff-Driven Timing Closure Methodology

This signoff timing-driven approach to timing closure first optimizes the design using physical implementation tools for critical scenarios. Implementation tools have the broadest set of optimization and transformation techniques to achieve the best possible quality of results. Signoff-accurate, physically-aware, all-scenario timing analysis is then used to complete final-stage ECOs in concert with place-and-route tools.

ECO Solutions Based on Timing Snapshots are Inadequate for Advanced Designs

Some design teams rely on ECO-specific tools to accelerate post-route design closure. Unfortunately, many of these ECO timing closure tools, even those designed specifically for the task, simply read in a snapshot of the timing data provided by signoff tools, and then suggest possible fixes based on simple estimation.

Today's designs can have millions of instances and numerous scenarios, which greatly increases the complexity of the ECO timing closure problem. When performing an ECO, timing estimation methods cannot properly estimate signoff timing effects such as signal integrity (SI), path-based analysis (PBA), waveform propagation, advanced on-chip variation (AOCV), or parametric on-chip variation (POCV). As a result, ECO solutions that rely on timing estimations or non-signoff timing engines are less predictable and often require additional iterations to close timing.

Signoff-Driven Timing Closure ECO Flow in the Synopsys Galaxy Platform

The ECO flow using IC Compiler, StarRC, and PrimeTime is shown in Figure 2. It provides the fastest path to signoff-driven timing closure.

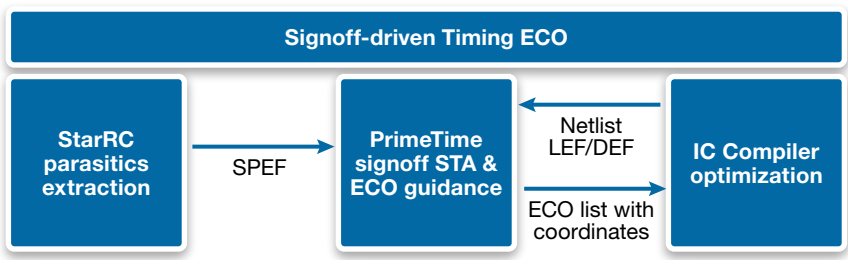


Figure 2: PrimeTime ECO Guidance in the Galaxy Platform

IC Compiler is a comprehensive physical implementation system that includes design planning, placement, clock synthesis, and routing for all technology nodes. It uses concurrent multicorner multimode optimization along with a powerful set of optimization capabilities to ensure best results with the fastest turnaround-time.

As designers complete the implementation phase and move into the timing closure phase, the benefits of using signoff-accurate timing and extraction tools for ECO guidance become increasingly more important. PrimeTime ECO guidance uses the accurate parasitics extracted by StarRC to create an ASCII Tcl-based change file for IC Compiler. This file is optimized for IC Compiler with physical location information and ensures feasibility for implementation.

This flow combines the high quality implementation from IC Compiler with the high capacity ECO guidance capabilities of PrimeTime to provide fast, accurate timing closure across all scenarios.

New Technology for ECO Guidance Delivers Scalable, Resource-Efficient Results

The new PrimeTime ECO guidance architecture is scalable across numerous scenarios in both runtime and capacity. This approach provides predictable results while delivering ECO guidance to implementation tools in a fast, memory efficient manner. PrimeTime ECO guidance uses the following patented technologies:

- ECO timing graph
- Composite graph view
- Calibrated estimation

The first new technology, the ECO timing graph, captures all related parts of the design, including violating endpoints and the slack values for these points. This compact graph is created quickly and efficiently for each scenario.

Violations are prioritized based on the relative criticality of the graph segments, each of which represents “per stage” slack values. This approach eliminates the need for iterative bottleneck analysis to determine the priority for fixing, enabling the process to complete quickly.

The second new technology, the composite graph view, is created from the individual timing graphs and provides a global view of all violations across all scenarios. The ECO algorithms reference this composite graph view to make fixing decisions for one scenario without affecting others.

The views shown in Figure 3, encompass all scenarios and enable a quick impact analysis of any proposed change on one scenario for their impact on others. This helps to avoid making recommendations that would later have to be retracted.

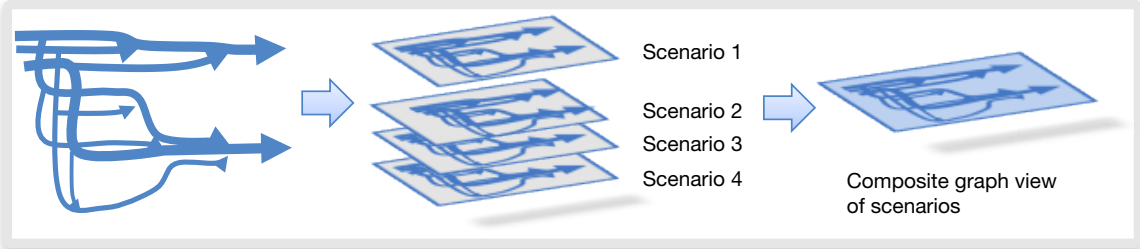


Figure 3: Composite Timing Graph Encompasses All Scenarios

The third innovation in PrimeTime ECO guidance is “calibrated estimation”. This technique quickly evaluates all available fixing options for a given timing violation and estimates the outcomes for all options without requiring a full timing analysis. It then calibrates the results with the signoff-accurate timing data from the “all-scenario” timing view, accounting for all analysis techniques including signal integrity, waveform propagation, and advanced on-chip variation effects. Figure 4 depicts the fast identification and selection of the best guidance decision for the device under consideration.

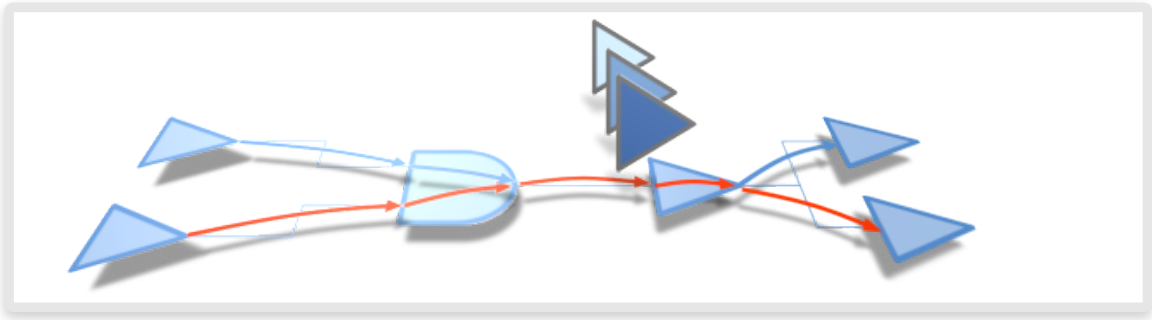


Figure 4: Calibrated Estimation

This approach is significantly faster than full timing analysis and improves the turnaround time per cell operation. By evaluating all possible guidance options across all scenarios quickly and efficiently, calibrated estimation enables highly predictable results with fewer changes to the netlist.

Physically-Aware Technology Reduces ECO Iterations

Placement and routing topologies of a design often present opportunities to achieve the best single-pass fix rate with minimal impact to the physical design. A new PrimeTime ECO technology deploys a lightweight physical interface that can populate the composite timing graph with physical information without affecting the tool performance or capacity.

With the available placement information, PrimeTime ECO can consider placement congestion and blockages and provide precise ECO guidance with location. Accurate ECO timing estimation can also be achieved by separating the original net parasitics based on the target location and recalculating cell and net delays as well as crosstalk effects. ECO guidance with location and accurate timing estimation ensures predictable signoff timing closure after implementation.

PrimeTime ECO also utilizes available space along the net route to increases success rates for ECO fixing in congested regions. Expanding the search space from the proximity of the driver or load pin to the entire net route vastly increases the possibility of an available space for buffer insertion. Figure 5 shows examples where placement-aware ECO:

- Prevents cell displacement by constraining cell upsizing to the available neighboring free space
- Recognizes placement blockage and inserts an ECO buffer on route

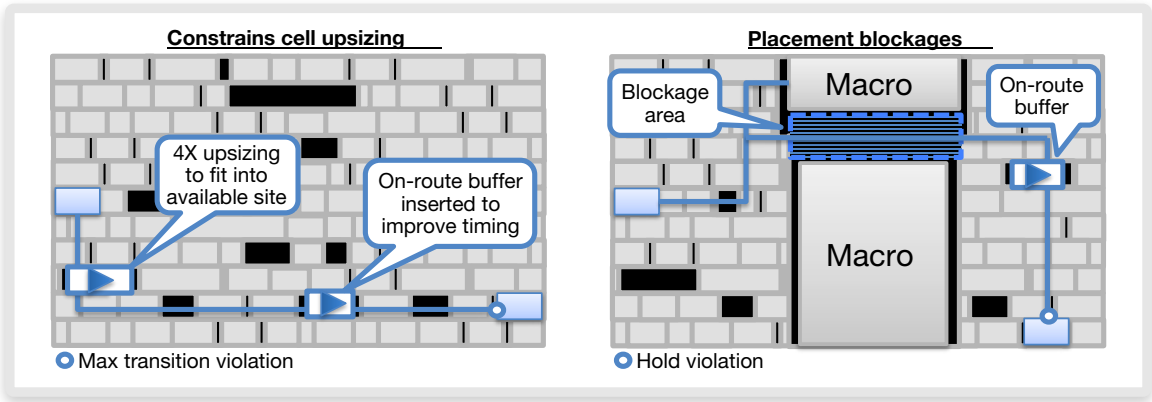


Figure 5: Predictable Results with Placement-Aware ECO

Furthermore, expanding the solution space onto the net route is critical for achieving the optimal fix for design rule violations. Inserting buffers along the net route is the most ideal method to improve DRC violations caused by long or high fanout nets. Figure 6 shows examples where routing-aware ECO can improve the fix rate and quality of results for max transition violations by inserting buffers according to the route topology.

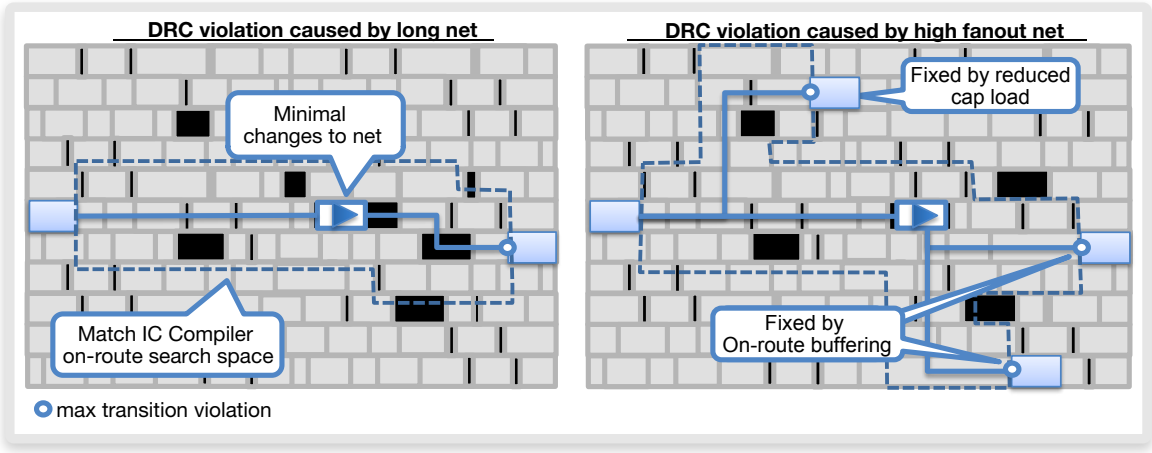


Figure 6: Improved Fix Rate with Routing-Aware ECO

For the most challenging timing violations where no single space is available around the target pins or along the route, instead of relying on the enormously time consuming process of manual fixing by the designer, PrimeTime generates ECO guidance with the location on a target path that has the lowest placement density. During the ECO implementation legalization step, the implementation tool can move cells in this local area to create available space for the ECO changes. Figure 7 shows an example where the ECO flow considers the placement density and successfully fixes violations with limited free space.

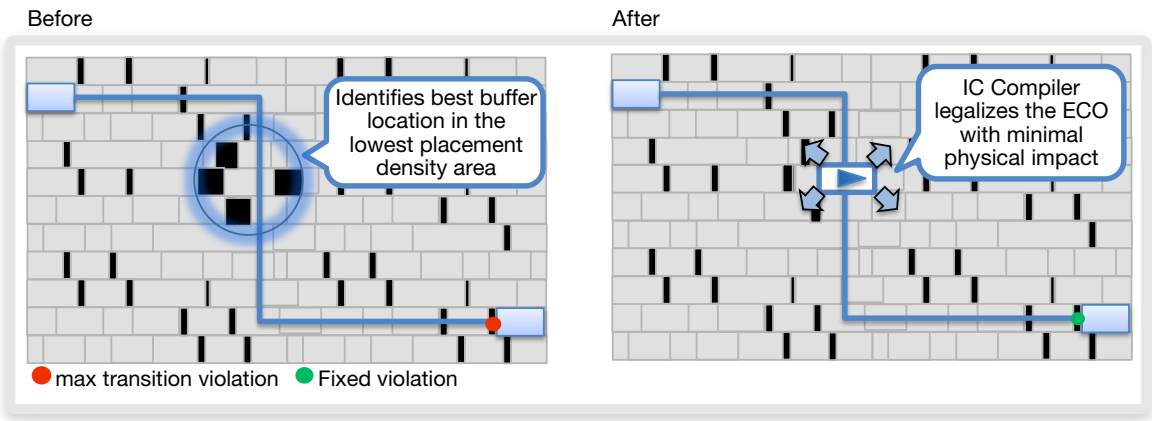


Figure 7: Placement Density-Aware ECO for Highly Congested Regions

While physically-aware ECO can take advantage of fixing opportunities on net routes, recognizing the voltage domain is critical for successful timing closure in advanced designs with complex voltage areas. In these designs, while driver and load pins can reside in the same voltage domain, the net route can travel through different voltage domains. Figure 8 shows an example where PrimeTime recognizes voltage areas in multivoltage designs and avoids ECO fixes that could introduce electrical rule violations.

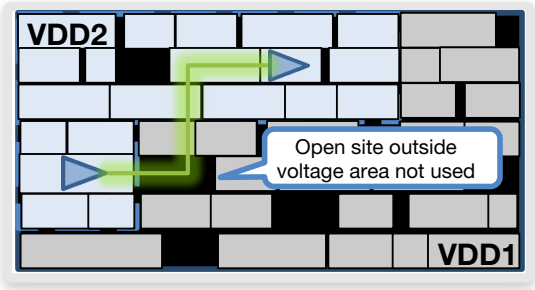


Figure 8: Voltage Area-Aware ECO for Multivoltage Designs

Recover Power and Area With Accurate Signoff Timing Analysis

Power consumption is a key factor of design quality, especially for energy-efficient designs that run on battery power. In the Galaxy implementation flow, you can apply power and area recovery technologies throughout the flow from logic synthesis to post-route optimization.

On timing paths with positive timing slack, power and area recovery technologies replace existing cells with lower power or smaller cells. Swapping existing cells with higher threshold voltage (Vth) cells induces no change to placement or routing while often reducing leakage power by orders of magnitude.† In addition, downsizing cells not only reduces dynamic and leakage power, it also frees up valuable space for other ECO opportunities, especially in highly utilized regions.

At the timing closure stage, PrimeTime uses various pessimism reduction technologies, including path-based analysis (PBA), waveform propagation analysis, and advanced and parametric on-chip variation technologies, to uncover additional recovery opportunities. Validating the ECO guidance using the signoff timing engine in all scenarios before submission is critical to ensure successful design closure and eliminate additional ECO iteration while achieving the best possible design quality.

ECO Implementation with Minimum Physical Impact

Routing changes during ECO implementation can introduce unexpected impact to signoff timing due to the change in wire load or crosstalk effects. In concert with PrimeTime physically-aware ECO guidance, which suggests ECO locations close to the target pin or original net route, IC Compiler's MPI technology preserves the majority of the original net route during ECO implementation, and restricts the route changes to only the local segment necessary for the newly inserted ECO cell.

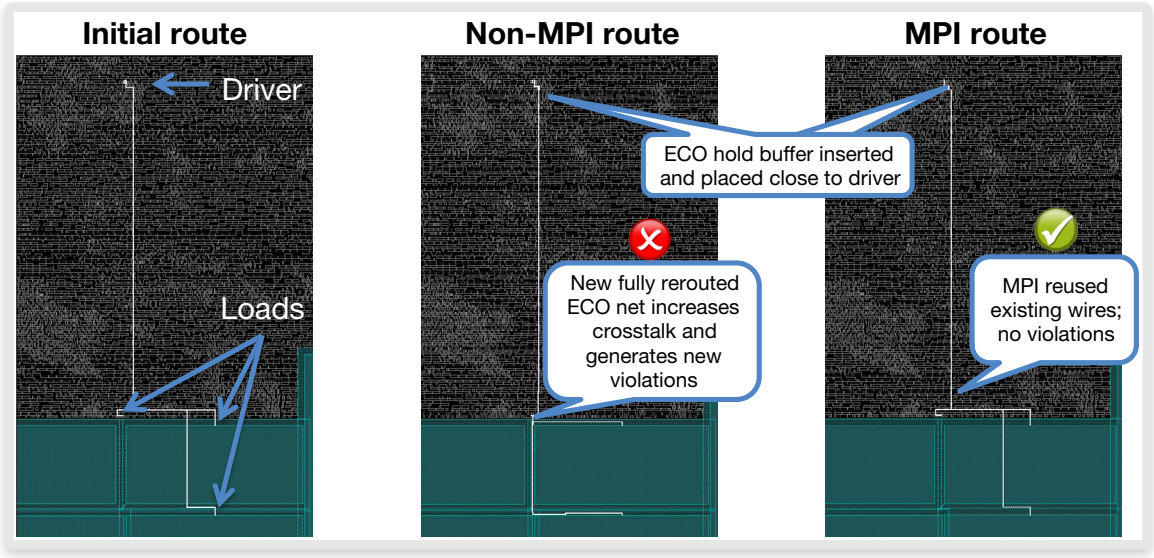


Figure 9: ECO Routing with IC Compiler MPI

By reusing the majority of the original net route, the change in wire load or crosstalk effects are minimal and highly predictable, ensuring timing closure after ECO implementation.

Furthermore, in congested regions, PrimeTime physically-aware ECO can take into account fragmented free spaces and placement density surrounding the target location when determining the feasibility of a new ECO cell. During ECO implementation, IC Compiler moves existing cells to consolidate the fragmented free spaces and accommodate the new ECO cell.

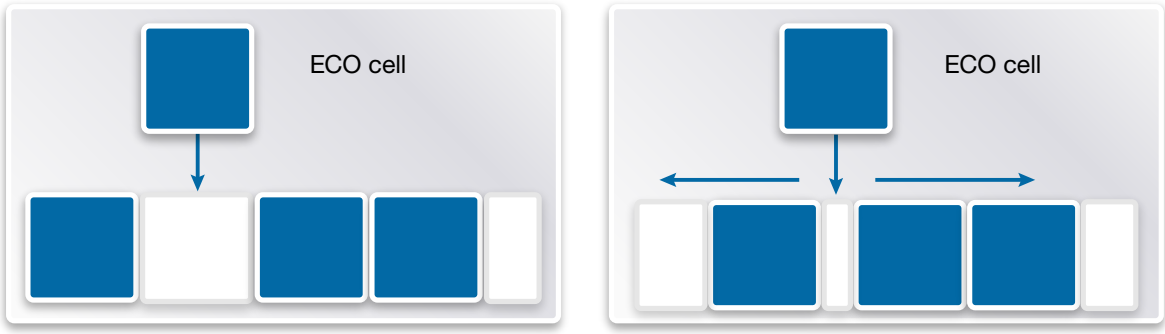


Figure 10: ECO Placement with IC Compiler MPI

PrimeTime physically-aware ECO can leverage the powerful incremental implementation engine in IC Compiler to accelerate signoff timing closure even on the most challenging designs.

PrimeTime Signoff-Driven ECO Guidance Results

The PrimeTime ECO Guidance Technology addresses the runtime and memory impact seen with increasing number of scenarios and accelerates timing closure by minimizing the number of ECO iterations.

Resource-Efficient Multi-Scenario ECO Guidance

As the number of scenarios increases with conventional ECO tools, the ECO runtimes grow at a nearly exponential rate. This is not the case with the new PrimeTime ECO Guidance algorithms, which minimally increase runtimes with scenarios, as shown in Figure 11.

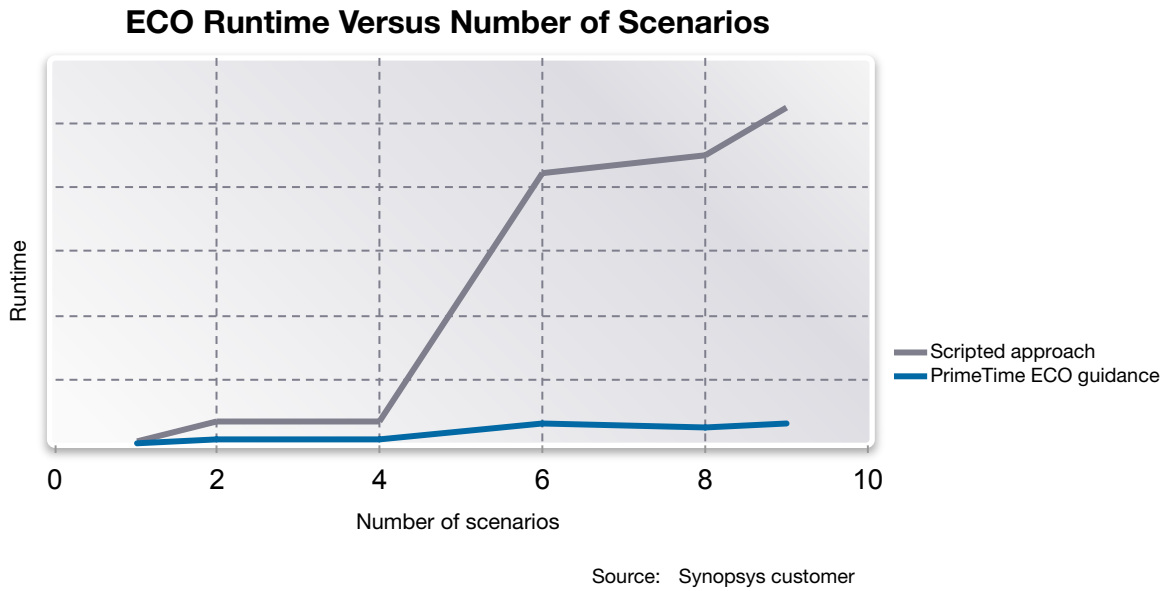
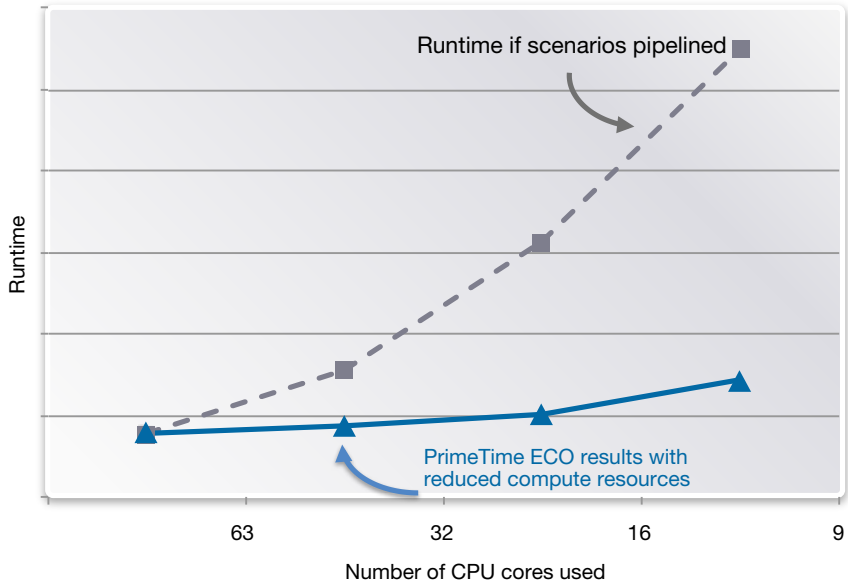


Figure 11: Scalability with Increasing Numbers of Scenarios

The combination of new timing graph ECO views and the calibrated estimation approach explained previously enables PrimeTime ECO Guidance to minimize the number of changes it recommends to the implementation tools. This approach avoids the creation of unnecessary congestion for the placement and routing tools, and contributes to the improved timing closure predictability.

Furthermore, PrimeTime ECO guidance runs efficiently even when the number of scenarios to be analyzed exceeds the number of processor cores available. An additional benefit of the “all-scenario” view of timing violations is the ability to run with fewer cores than the number of scenarios at the same fix rate.

Figure 12 shows the results of an ECO run where the theoretical time required for ECO guidance to run 63 scenarios is plotted on the upper gray line. As the number of CPU cores is reduced from 63 to 32 to 9 cores, the runtime increases dramatically. The lower blue line shows the new ECO guidance runtime as resources are similarly reduced. Even with seven times fewer resources, the impact on performance is minimal with the runtime increasing less than two times while maintaining a high success rate for this reduced-resource run; there was no impact to the quality of results, and 96% of the hold violations were fixed in a single pass in this customer test case, identical to that when utilizing the full number of CPU cores.



Source: Synopsys customer design

Figure 12: Resource-Efficient Approach When Scenarios Exceed Hosts

Predictable Timing Closure With Physically-Aware Technology

Physically-aware ECO guidance minimizes layout perturbation during ECO implementation to achieve predictable timing closure. Figure 13 shows the results from Synopsys customer designs that used ECO guidance implementation by IC Compiler. These customer test cases show very high single-pass fix rates for DRC, setup, and hold violations.

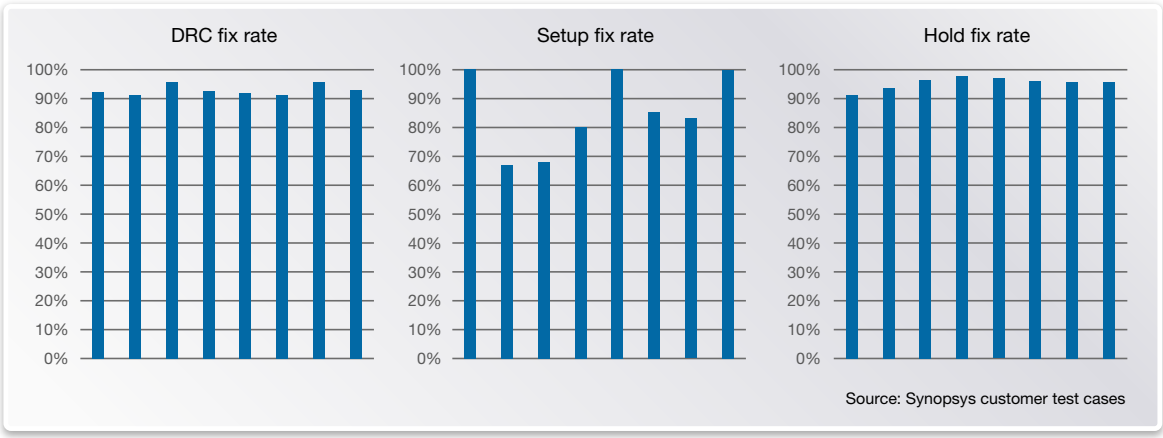


Figure 13: Predictable Results Through Place and Route

ECO guidance fix rate compares timing before ECO guidance to remaining violations after the PrimeTime ECO guidance is implemented in IC Compiler and brought back into PrimeTime with StarRC parasitic extraction.

Leakage Recovery with IC Compiler and PrimeTime

The amount of leakage recovery achievable after timing closure is mainly dependent on the amount of power optimization efforts already spent during the implementation flow. Figure 14 shows that PrimeTime can reduce a noticeable amount of leakage power in various customer cases that deployed leakage recovery technologies in IC Compiler.

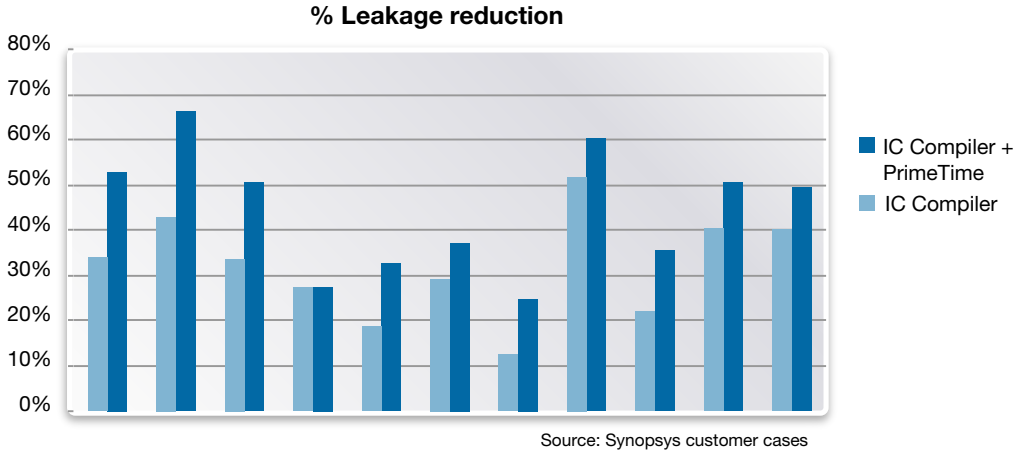


Figure 14: Additional Leakage Power Recovery After Timing Closure

Summary

New technologies in PrimeTime deliver a scalable, effective, signoff-accurate methodology to close timing across all scenarios. The use of PrimeTime physically-aware ECO guidance improves single-pass fix rate and ensures predictable implementation results. Together with new technologies in IC Compiler, PrimeTime signoff-driven ECO guidance eliminates costly ECO iterations and accelerates timing closure and signoff.

Reference

- PrimeTime ECO Guidance Technology Page on Synopsys.com
- SolvNet Documentation: PrimeTime User Guide Contents (see PrimeTime ECO Guidance Technology
- SolvNet articles with additional reference links:
  - SolvNet article 033465, "Save Weeks Fixing ECOs with PrimeTime and IC Compiler"
  - SolvNet article 035247, "Close ECO Timing Faster with New PrimeTime DRC Guidance"
  - SolvNet article 039613, "PrimeTime SIG at DAC 2013 - Technology Panel - Advanced ECO Methodology"

†Source: Synopsys internal testing

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