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Predictable Success

Synopsys and STMicroelectronics

High-Level Synthesis Flow Achieves Higher Reliability and Productivity for Multi-rate Digital IF TV ASIC

Synphony Model Compiler really improved our productivity and reliability in designing complex multi-rate DSP algorithm, mixed-signal functions and generated very reliable results."

François Rémond
CAD & Design Methodology Director, Home Entertainment & Displays Group, STMicroelectronics

Business

STMicroelectronics is a global semiconductor company producing a diverse range of devices, ranging from single transistors to microprocessors and complex SoCs. The Home Entertainment and Displays (HED) Group is a leader in multimedia convergence solutions.

Challenges

- Improve productivity for complex multi-rate digital signal processing (DSP) algorithms such as demodulation
- Quickly explore architecture tradeoffs
- Deliver at-speed FPGA prototype early in the design flow for algorithm validation
- Generate unique RTL for FPGA and ASIC with more confidence
- Quickly implement and verify design in a standard RTL ASIC flow
- Fast turnaround from algorithm to real-time FPGA verification

System-Level Design Solutions

- Synphony Model Compiler tool and models
- Synplify Premier FPGA logic synthesis

Benefits

- Fast ramp up and ease of use with high-quality Synphony Model Compiler IP model library
- Integrated digital and mixed-signal model simulation
- Easy model definition of the demodulator using flexible schematic capture
- Better exploration of the DSP algorithm at a high level
- Delivered multi-rate FPGA prototype months sooner
- Achieved 160MHz operating frequency in the FPGA prototype allowing "at speed" design validation
- Easily target design from FPGA to ASIC using high-level synthesis
- Automatic RTL code generation for reliable IP delivery and automatic testbench generation for verification

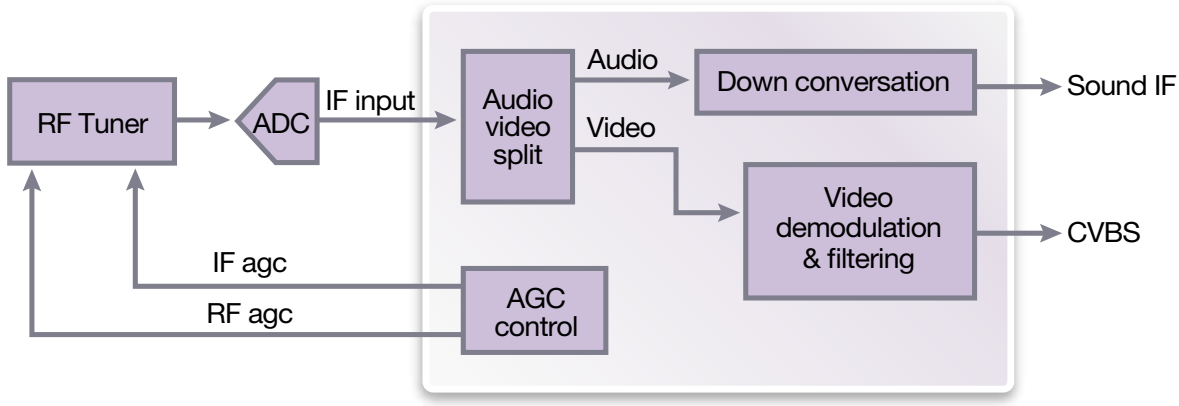

Figure 1: Digital Intermediate Frequency (DIF)

Overview

STMicroelectronics' Home Entertainment and Displays (HED) team focuses on next-generation technology for home video and integrated silicon solutions, audio, and TV and monitor. Examples include high-definition DVD, digital audio amplification and Internet TV.

These ASIC designs include a large amount of complex, real-time digital signal processing algorithms. In order to speed up the development cycle and allow a comprehensive validation of their digital IF TV demodulator ASIC (called DIF), ST needed a complete synthesis flow, that could feed optimized RTL created from high-level models to an FPGA prototype for validation of their ASIC, before retargeting the RTL to the final ASIC.

Rapid Algorithm Design and Exploration

The DIF IP used in ST's HED products had an intermediate frequency input sampled at 160 MHz, 4 digital mixers, 2 PLL, and 15 filters including 2 down-sampling converters and 1 sampling rate converter (SRC) with more than 1250 taps. Three mixed-signal AGC controls added complexity to this design.

The team used Synphony Model Compiler to specify multi-rate, high-speed video and audio demodulation in the Simulink model-based design environment. Synphony provided an IP model library that facilitated rapid design of synthesizable algorithms that were also technology independent. Simulink also supported continuous-time analog models which allowed comprehensive verification at a high abstraction level. Using Synphony's high-level compiler, designs could be optimized by exploring different architectures and could target a variety of FPGA and ASIC devices. Thus, a single model can be used to drive both FPGA and ASIC flows without breaking the verification continuity.

Synphony models allowed easy refinement of the algorithms used in this design with its automatic or user-controlled datatype propagation. Vector signals allowed concise description of the desired

"We were able to ramp up our design prototype very early and could iterate quickly with this high-level synthesis flow. The flow allowed us to cut months off our schedule. Using Synphony Model Compiler, we could explore the results of using different architectures. Using Synplify Premier we quickly obtained a high-performance FPGA prototype."

Christine Masson
Signal Processing Sr. Designer, TV & Monitor Division, STMicroelectronics

parallelism. Additionally, STMicroelectronics could make their own parameterisable custom blocks and save these blocks as libraries for future re-use.

Early FPGA Prototyping

Using a complete high-level synthesis flow with SynphonyModel Compiler and Synplify Premier, STMicroelectronics was able to deliver a full-speed, multi-rate FPGA prototype cutting months off the project schedule. This was enabled using a tightly-integrated flow comprised of high-level synthesis, FPGA technology characterization, and FPGA logic synthesis. The team implemented and validated their complex design in a tight timeframe with a reduced design team. Using Synphony MC and Synplify Premier, they could perform rapid iterations, explore architectural tradeoffs and rapidly incorporate specification changes.

Synopsys' Synphony Model Compiler eliminated coding and verification efforts by easily translating design intent into high quality-of-results RTL for use with both ASIC and FPGA tools.

The entire design flow benefited from faster turnaround time helping the team quickly implement changes, working at a high level of abstraction.

Unlike other HLS and logic synthesis flows, the Synopsys flow includes a multi-rate IP model library that can be used across multiple clock domains.

Reliable ASIC Flow Integration

Synphony Model Compiler was able to quickly generate an optimized architecture for ST's 65nm ASIC technology and generate high-quality RTL that passed verification tapeout guidelines. The IP has 27,000 registers, 0.89 mm2.

Synphony Model Compiler reduced schedule risk during the entire development flow. Its automatic RTL testbench generator created testbenches that guaranteed the equivalence of the design from the Synphony model description down to the ASIC or FPGA netlist.

ST's Home Entertainment and Displays Group digital intermediate frequency (DIF) demodulator ASSP was introduced and quickly integrated into several products. With this project behind them, ST's HED group is well on its way to developing the next-generation of multimedia convergence technology solutions.