

# Synopsys and IMEC

## IMEC Surpasses Critical Performance Goal for C-Programmable Multimedia ADRES Processor with Synplify



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**Maryse Wouters**

Activity Leader of the Integration Team, IMEC

### Summary

IMEC, a European nanoelectronics research institution, used Synplify® Premier software from Synopsys to demonstrate that its C-programmable reconfigurable processor architecture, ADRES, is feasible for use in portable wireless multimedia devices. The entire processor system was successfully prototyped for a multimedia ADRES processor instance on a Xilinx Virtex®-4 FPGA through use of the Synplify Premier tool. The Synplify Premier product provided excellent support for achieving the required clock frequency. IMEC credits the Synplify Premier tool's built-in knowledge of the FPGA's physical characteristics for the accurate timing results that it delivers. The ADRES prototype system has been important for IMEC in showing that the ADRES processor architectural template and its corresponding C-compiler are sufficiently stable for use in portable devices.

### IMEC's ADRES Innovation Promises a New Future for Handheld Multimedia Devices

IMEC of Leuven, Belgium is one of the world's leading independent research institutions in nanoelectronics and nanotechnology. Its research focuses on next-generation chips and systems, and bridges the gap between university research and

technology development in industry. IMEC's blend of know-how and corporate relationships position the organization to help shape key technologies for future systems.

ADRES (Architecture for Dynamically Reconfigurable Embedded Systems) contains two views which are tightly coupled: an array of processing elements that runs the data flow part of the application and a VLIW that executes the control. For handheld multimedia devices, this technology delivers enormous flexibility benefits over fixed ASICs because various video codec standards can be quickly and easily accommodated through C programming. In addition, ADRES-based processors offer power efficiencies six to twelve times higher than state-of-the-art C-programmed processors.

With the demonstration, IMEC has proven that processors based on the ADRES architecture can deliver sufficient performance. The multimedia ADRES processor instance was developed to support MPEG-2, MPEG-4 and H.264/AVC video decoding at resolutions ranging from QVGA up to D1. The demonstration employed a HAPS-32 prototyping board, which contains two Xilinx Virtex-4 LX200 FPGAs. IMEC constrained the FPGA clock input to 50 MHz to decode 30 frames/sec of H.264/AVC content at CIF resolution.



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### **Synplify Premier Tool Delivers the Necessary Performance**

IMEC began by synthesizing the design using the Synplify Pro® product from Synopsys, a tool that had served the organization well for many years. Synplify Pro software came close to the goal at 46 MHz, but not close enough.

“It was essential that we find a way to reach 50 MHz, and so we performed an investigation of the state of the art in FPGA synthesis,” said Maryse Wouters, Activity Leader of the Integration Team. “Fortunately we found our answer, the Synplify Premier solution, which is capable of delivering the performance we needed. In fact it did even better than we had hoped, 52.6 MHz. Everyone was pleased with the performance gain.”

“The reason why the Synplify Premier tool does the job better is that it understands the physical characteristics of the FPGA in fine detail and uses that knowledge to craft an optimal design,” explained Wouters. “That’s particularly important with the most advanced FPGAs on the market.”

Building on Synplify Pro technology, the Synplify Premier solution embodies its knowledge of an FPGA’s specifics through a patented technique called graph-based physical synthesis, which represents an FPGA’s pre-existing wires, switches, and placement sites as a detailed routing resource graph. Graph-based physical synthesis produces rapid timing closure by automatically outputting timing-correlated legal placement and by considering availability of actual FPGA routing resources when measuring delays, rather than just physical proximity of instances. Unlike ASICs, in an FPGA physical proximity does not always correlate to timing delays, making ASIC-style physical synthesis approaches inaccurate when applied to FPGAs. Only graph-based physical synthesis can

accurately estimate timing delays when performing physical synthesis.

Graph-based physical synthesis also cut place-and-route runtimes significantly for IMEC. The total elapsed time for placement and routing was six hours with the Synplify Premier physical synthesis solution versus seventeen hours with a logic synthesis tool. The reason is that in addition to performing synthesis, the Synplify Premier product actually places the design in a manner known to meet timing, and delivers a design that will be fully routable using the Xilinx ISE toolset.

The correlation between the Synplify Premier solution’s performance predictions and actuals was much better than IMEC had seen. The new tool predicted 51 MHz performance, which was very close to the actual result of 52.6 MHz.

### **IMEC’s New Standard for Synthesizing 90-nm FPGAs and Below**

With its flexibility to incorporate multiple video codec standards, the short time-to-market made possible by its high level language programmability, and its power efficiency, ADRES promises to play a major role in the next generation of mobile multimedia platforms.

“Using an FPGA-based prototype platform, IMEC has demonstrated its C-programmable multimedia ADRES processor instance for real time H.264/AVC video decoding,” said Wouters. “The performance gain that the Synplify Premier solution delivered was as promised in the Synplify Premier data sheet.”

Because of the excellent results it delivers, the Synplify Premier product has now become part of the tool flow at IMEC for future projects using leading edge FPGAs. “It is clear that for 90-nm FPGAs and beyond, the timing closure offered by the Synplify Premier tool is crucial,” Wouters concluded.