

Wilocity Teams with Synopsys

Synopsys Professional Services Integrates DesignWare IP for 65nm Wireless PCI Express Design



As consumers demand greater mobility, device manufacturers are requiring advanced mobile computing platforms that enable them to deliver thin and light devices without sacrificing performance and functionality. Wilocity's use of proven DesignWare IP and close collaboration with Synopsys Professional Services has enabled us to successfully develop truly multi-gigabit wireless chips that are optimized for today's mobile devices."



Ido Naishtein
 Director of Physical Design, Wilocity

Overview

Founded in March 2007, Wilocity provides 60 GHz Wireless PCI Express solutions for the mobile computing and computer peripherals markets. Their newest SoC is based on the Wireless Gigabit Alliance (WiGig) and IEEE802.11ad draft specifications, enabling multi-gigabit wireless for a wide range of applications, from I/O to networking to video. Wilocity engaged Synopsys Professional Services to assist with design flow development and physical implementation. Collaboration initially aimed at lowering power consumption led to improved architectural partitioning and advanced algorithm implementation, culminating into a complete and optimized RTL to GDSII chip implementation that included silicon-proven DesignWare IP.

Synopsys Solution

- ▶ Synopsys Professional Services
- ▶ DesignWare[®] IP for PCI Express[®] 2.0, embedded memories and logic libraries
- ▶ Galaxy[™] Implementation Platform

Cooperation Benefits

Synopsys teamed with Wilocity to deliver the expertise of an experienced design consulting team while dynamically balancing resource needs throughout the entire design process, resulting in a successful tape-out. In addition, Synopsys provided Wilocity with IP for the SoC, including PCI Express, embedded memories and logic libraries, all optimized for performance, power and area. By leveraging the breadth of Synopsys' DesignWare IP solutions and expertise from Synopsys Professional Services, Wilocity was able to reduce power consumption, in some of the more complex arithmetic clusters, by approximately 50 percent, increase performance by 65 percent and improve utilization by up to 70 percent.