

Synopsys and Verayo

Verayo Achieves First-Pass Silicon Success for RFID Security IC with DesignWare AEON NVM IP



Synopsys was the only provider to offer a silicon-proven MTP NVM IP solution that met all of our performance, power and cost requirements and was easily ported to the targeted process technology.”



Richard Sowell
 Director of Engineering, Verayo

Business

Verayo builds security and authentication solutions based on Silicon Physical Unclonable Functions (PUF) technology. Since its founding, the Verayo team has designed and tested integrated circuits (ICs) using PUF technology, building a substantive know-how beyond the initial IP that Verayo licensed exclusively from MIT.

Challenges

- ▶ Acquire proven NVM IP solution to meet the operating requirements of an RFID environment, including power and area constraints
- ▶ Obtain complete design views, documentation and knowledgeable support to reduce integration risk
- ▶ Meet aggressive time-to-market schedule
- ▶ Available in a low cost semiconductor process

DesignWare® IP Solution

- ▶ AEON® Multi-time Programmable (MTP) Non-volatile Memory (NVM) IP

Benefits

- ▶ Acquired a silicon-proven NVM IP solution that met stringent cost and design requirements
- ▶ Received training and excellent technical support during the integration process
- ▶ Achieved first-pass silicon success and met time-to-market window

Overview

Verayo is focused on building security and authentication solutions based on PUF technology. This technology brings three fundamental capabilities to semiconductor ICs:

- ▶ It makes ICs effectively unclonable by implementing electronic DNA in silicon
- ▶ It makes it possible to securely authenticate any IC
- ▶ It can generate a virtually unlimited number of unique cryptographic root master keys from each IC.

The small PUF circuits are uniquely suited to RFID devices that have cost and power-consumption constraints. Verayo is harnessing PUFs to provide the best level of security for authentication applications leveraging RFIDs to four solutions in the market, including:

- ▶ Unclonable PUF-based ICs (RFIDs initially) for anti-counterfeiting
- ▶ Modular authentication software solutions to authenticate PUF-based ICs
- ▶ PUF-based crypto platforms for secure authentication & transaction processing
- ▶ Secure processors for general purpose “trusted computing” applications.



Synopsys' proactiveness was instrumental in getting our chip out on time. Kudos to the Synopsys team for supporting us in a very responsive way, allowing us to meet our tight time-to-market window."

Richard Sowell

Director of Engineering, Verayo

Leading DesignWare IP Solution

Targeted for use in mobile applications like Near Field Communication (NFC) devices, Verayo's Vera M1 PUF-based RFID mixed-signal IC had to incorporate non-volatile memory (NVM) IP for read/write capabilities. Verayo had specific criteria to meet in their IP selection process. The IP they chose had to meet the operating requirements of an RFID environment, including power and area constraints. Also, with their design based on a 180-nm process technology, Verayo needed IP that could be implemented on the same node. One of the IP providers being considered would have required Verayo to port their design to that provider's process, which would make Verayo's own existing IP unusable. Verayo's preferred option was to choose a vendor that could quickly and easily port the IP to their required node without causing delays and jeopardizing their tight deadline.

Synopsys' DesignWare AEON NVM IP is optimized for power and meets the needs of high-frequency (HF) passive RFID tags in the industry's most cost-effective RF processes, which proved to be an excellent solution for Verayo. The congruence of Synopsys' trusted NVM IP solution with Verayo's requirement for reduced area as a cost consideration, high performance (up to 10k write cycle endurance) and low-power consumption resulted in a very efficient solution for Verayo. In addition, Synopsys' industry-proven NVM IP had been ported to nodes similar to Verayo's required node, reducing performance and schedule risks for the new port.

High-Quality IP and Excellent Support

Synopsys' high-quality, silicon-proven DesignWare AEON NVM IP helped ensure that Verayo's design would work right the first time.

Synopsys' willingness to port the IP to the required process technology enabled Verayo to reuse their previous design, further saving time and rework. Additionally, a third party performed final integration of the chip for Verayo, so Synopsys worked with Verayo's engineering team as well as the third party to ensure delivery of a high-quality design. "The Synopsys IP team had insight into what was needed; they quickly evaluated the requirements to port their IP and provided support all the way through integration," said Richard Sowell, director of engineering at Verayo.

Synopsys' comprehensive product documentation and knowledgeable and responsive technical support team eased Verayo's integration of the DesignWare AEON MTP NVM and helped Verayo achieve first-pass silicon success in its mixed-signal design. "We're extremely satisfied with the performance and quality of the Synopsys IP in our device, and we hope to continue our relationship with Synopsys on future projects," said Richard Sowell, director of engineering at Verayo.

"Synopsys' high-quality DesignWare AEON MTP NVM IP required minimal integration effort onto the SoC, enabling us to deliver a right-first-time design."



Richard Sowell

Director of Engineering, Verayo



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