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Predictable Success

Synopsys and PLX Technology

PLX First to Market with PCI Express Gen 3 Switch using DesignWare Embedded Memory IP

After qualifying several vendors, we found Synopsys' silicon-proven DesignWare Embedded Memory portfolio offered the broadest range of compilers with an array of options to meet our varied design requirements. The combination of small area, high performance and advanced power management capabilities made selecting Synopsys an easy choice."

Syed Ahmed,
Senior Director of Physical Design, PLX Technology

Business

PLX is the technology leader in PCI Express switches, bridges and 10GBase-T PHY solutions, with additional leadership in consumer storage controllers as well as general purpose USB controllers. As these serial technologies have become mainstream, PLX has been able to offer differentiated products that provide scalability and performance at a low cost.

Challenges

- Meet aggressive time-to-market schedule for new PCI Express Gen 3 switch design
- Reliably achieve high-performance, with low power dissipation and small area on an advanced node
- Implement an embedded memory IP solution with integrated test and repair capability

DesignWare IP Solution

- 40-nm Embedded Memory compilers
- STAR Memory System test and repair solution

Benefits

- Achieved first-pass silicon success and met first-to-market goal
- Obtained silicon-proven embedded memory compilers that demonstrated consistent and reliable on-chip performance with low power dissipation
- Utilized unique integrated test and repair system to improve manufacturing yield

Overview

PLX supplies high-performance, low-power system-interconnect silicon-based semiconductors and firmware for the enterprise communications, storage, server, compute, embedded-control and consumer storage markets. PLX's serial protocol solutions include technology based on 10 Gigabit Ethernet, PCI Express®, USB and SATA interfaces.

PLX's ExpressLane™ PCI Express (PCIe) product family, compliant with the PCI Express base specifications, offers fully configurable switches with non-transparent bridge function and forward/reverse bridges. These solutions range from the industry's

Synopsys is an IP vendor that aggressively addresses issues; Synopsys' technical support team was very in tune with our needs at every step of the design process and quickly resolved any issues that arose."

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largest, most versatile switch at 96 lanes and 24 ports, to a three-lane, three-port switch for more streamlined designs. PLX offers valuable features to support their customers' needs for performance and fast time to market including:

- Highly flexible port configurations
- Low latency transfers
- Non-transparent port capability
- Host-centric and true peer-to-peer data transfers
- Industry's lowest power and smallest footprint

First to market with PCIe switches in 2004, PLX continues to expand its portfolio with its PCIe Gen 3 switch family, ranging from 12 to 48 lanes. Board and system designers can take full advantage of the latest PCIe specification's bidirectional 8Gbp/s per lane, which enables one PLX 48-lane Gen 3 switch to handle 96Gbp/s of full-duplex peer-to-peer bandwidth.

Leading DesignWare IP Solution

PLX ExpressLane PCIe Gen 3 Switches bring to the market speed and performance with low power. Offering multi-host PCI Express switching capability, PLX's PCIe Gen 3 Switch targets enterprise and home-based applications requiring high-bandwidth data transfer, low latency, low power consumption, integrated hot-plug support, small footprint and highly flexible configurations.

With a large percentage of their 30 million-gate SoC consisting of SRAMs, PLX needed a high-quality embedded memory IP solution that offered a robust, integrated test and repair capability, high performance on an advanced 40-nm process, and the smallest area. In addition, with the goal of being first to market with the PCIe Gen 3 switch solution, PLX needed an IP vendor that had the expertise and support infrastructure to help meet their aggressive project schedule. After evaluating several IP providers based on these criteria, PLX selected Synopsys.

Synopsys provided PLX with a broad range of high-density and high-speed memory compilers that incorporate advanced power management features including light sleep, deep sleep, shut down and dual power rails, enabling PLX to choose the right solution optimized for their specific needs. "The variety of memory options made it very easy for us to optimize our design. We knew we could meet our area and power requirements and because of our past relationship with Synopsys, we were confident the product would be of good quality," said Syed Ahmed, senior director of physical design, PLX Technology.

"We were very impressed with the test and repair functionality in the DesignWare Embedded Memory solution. Having a built-in self test solution allowed us to lower our overall chip area and cost. We also made extensive use of the built-in diagnostic capability of the STAR Memory System's Silicon Browser component, which enabled us to quickly get to working silicon and accelerated time-to-manufacturing.

Syed Ahmed,
Senior Director of Physical Design, PLX Technology

High-Quality IP and Excellent Support

Synopsys' high-quality, silicon-proven 40-nm embedded memories were a low-risk, easy-to-integrate solution for PLX, and the responsiveness of Synopsys' support team ensured efficient and timely resolution of issues. "Synopsys' knowledgeable support team went above and beyond the call of duty in the speed with which they synced up with revisions of the 40-nm process technology," said Syed Ahmed, senior director of physical design, PLX Technology.

The DesignWare STAR Memory System integrated test and repair solution was another benefit for PLX. Since a significant portion of the chip consisted of SRAMs, they needed a high quality test and repair capability that would identify and resolve manufacturing faults, leaving nothing to chance. "The unique test and repair capability of the STAR Memory System, combined with the predictable performance of Synopsys' embedded memory enabled us to easily integrate the IP into our design within a couple of weeks, and we had no surprises at tape-out," said Syed Ahmed, senior director of physical design, PLX Technology.

With the success of their PCIe Gen 3 Switch well underway, PLX is looking forward to their next-generation of ExpressLane PCIe Switch products, and plan to continue to use DesignWare IP.

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