

Synopsys and PLSense

PLSense Achieves 0.45V Operation With Sub-Threshold Technology Implemented on Synopsys' ARC Data Fusion IP Subsystem



“We needed a processor solution that would support extremely low-power operation for our sub-threshold SoC solution. Synopsys' DesignWare ARC Data Fusion IP Subsystem supported our low power requirements while delivering excellent performance.”—Uzi Zangi, CEO, PLSense

Business

PLSense provides an integrated, general-purpose ultra-low power MCU chip solution that achieves minimum energy per operation for the targeted performance in a wide range of frequencies (up to 100MHz) required by battery-operated IoT applications. PLSense delivers a complete sub-threshold solution that extends system battery life by 5 to 10X compared to other solutions available today.

Challenges

- ▶ Deliver reliable, sub-threshold, ultra-low power solution for battery-operated IoT applications
- ▶ Implement a new, complete solution and libraries for sub-threshold voltage use

Synopsys Solution

- ▶ DesignWare[®] ARC[®] Data Fusion IP Subsystem with ARC EM5D Processor
- ▶ ARC MetaWare Toolkit and ARChitect configuration tool

Benefits

- ▶ Achieved first-pass silicon success for sub-threshold voltage chip, with operation as low as 0.45V
- ▶ Eased integration with silicon-proven ARC processors and tools

Overview

PLSense has developed the PLS10 MCU to address the lower power consumption and extended battery life requirements of IoT applications. The PLS10 is an integrated, general-purpose, ultra-low power MCU that includes support for a full range of DSP functions, full DMA functionality and a broad range of interface options. It utilizes the company's unique near/sub-threshold technology including the Adaptive Dynamic Voltage Control (ADVC) mechanism, which enables a 3 to 7X reduction in power compared to other MCUs with similar functionality. The PLS10 can be connected directly to a battery source and operates from internally-generated voltages between 0.45V and 1.1V. In order for PLSense to deliver an MCU that would operate at sub-threshold voltages, all the components of the solution need to support low-voltage operation as well. Because not all designs support sub-threshold operation, many elements need to be newly built from the transistor level. It was important that PLSense find an architecture that would support their ultra-low power design.

“Lowering operating voltages in order to achieve ultra-low power designs is a major challenge since not all existing implementations will work at these sub-threshold voltages. The ARC MetaWare Development Toolkit was easy to use, saving us time on the IP design and integration, allowing us to focus on other elements of our design, including building the sub-threshold libraries and technology.”—Uzi Zangi, CEO, PLSense

DesignWare ARC Processors and Development Tools

Synopsys' ARC Data Fusion IP Subsystem specifically targets always-on IoT applications, delivering excellent performance while adhering to the constrained power envelope of a battery operated device. The ARC Data Fusion Subsystem eases integration effort while reducing on-chip latency and energy consumption compared to typical bus-based systems and enabled PLSense to:

- ▶ Quickly and easily integrate their design and achieve first-pass silicon success
- ▶ Implement their low-voltage design while achieving required performance
- ▶ Save development time and effort leveraging MetaWare Development Toolkit
- ▶ Leverage the configurability and extensibility of the core and subsystem to achieve optimal performance within stringent power requirements

Using the ARC EM5D processor-based ARC Data Fusion IP Subsystem and MetaWare Development Toolkit, PLSense quickly and easily integrated their design and achieved first-pass silicon success. PLSense intends to continue using ARC processors and subsystems in future designs.