Synopsys and Marvell
Marvell Reduces Networking SoC Die Size by 10% With DesignWare STAR Memory System Multi-Memory Bus Processor

"Synopsys’ STAR Memory System and Multi-Memory Bus Processor is unique to the industry. No competitive solution can match its flexibility, high test coverage, and ability to minimize test area, power and cost."

Gevorg Torjyan
Principal Architect, Marvell Semiconductor, Inc.

Business
A leading fabless semiconductor company, Marvell provides expertise in microprocessor architecture and digital signal processing that drives high-volume storage solutions, mobile and wireless, networking, and consumer products. Marvell’s networking search engine product line delivers high capacity, fast performance and low power consumption for mobile and Internet of Things (IoT) applications.

Challenges
- Maintain high standards for timing and performance
- Realize comprehensive memory test coverage and implement effective repair solution for increased yield
- Reduce area of networking system-on-chip (SoC)

DesignWare IP Solution
- DesignWare® STAR Memory System including
  - Multi-Memory Bus (MMB) processor
  - Yield Accelerator

Benefits
- Reduced SoC die size by 10% using multi-memory bus processor with no performance impact
- Quickly and efficiently generated test vectors to reduce silicon bring-up time and minimize test engineering effort
- Received excellent, responsive technical support from an expert team

Overview
Marvell’s networking technology supports the explosive growth of mobile devices, IoT and automotive connectivity while addressing the future scaling requirements of both bandwidth and service density from a system cost, power, form-factor and reliability perspective. Marvell’s products help carriers and service providers introduce, manage and rapidly scale new revenue-generating services while offering enhanced security and network quality.

Marvell’s latest custom memory SoC is designed to increase the search capability of routers. With a design of this complexity, Marvell required a memory test and repair solution that would allow it to meet its timing requirements and achieve high quality test coverage while minimizing the test area overhead. Marvell’s SoC includes more than 7,500 memory instances in which a traditional built-in-self-test (BIST) implementation would require test wrappers around every memory instance, increasing overall area and routing congestion. To avoid these issues, Marvell required an area-efficient memory test and repair solution. In addition, Marvell needed to use its engineering resources on product differentiation and automate otherwise tedious vector development.
“With a project this big, test automation was critical. Only Synopsys’ STAR Memory System gave our team the confidence to focus on product differentiation and leave the BIST to a third-party tool.

Sohail Syed
Sr. Director of Engineering, Marvell Semiconductor, Inc.