SYNOPSYS®
Silicon to Software™

Synopsys and Fuji Xerox

Fuji Xerox Develops Scanned Image Data Processing ASIP for Full-Color Digital Multifunction Device Using Synopsys ASIP Designer

By using Synopsys' ASIP Designer tool, we were able to reduce gate count by 70%, which enabled us to implement our design in an FPGA and retain the required system performance of printing 70 pages a minute with our multifunction printer."

Noriaki Tsuchiya
Manager, Controller Development Group, Fuji Xerox

Business

Fuji Xerox Co., Ltd. is a major office automation product supplier in Japan, providing document services and solutions centered on digital color/monochrome multifunction office devices.

Challenges

- Reduce gate count for their multi-function printer while meeting target performance goals
- Reduce system development cost
- Flexibility to avoid design respins

Synopsys Solution

- ASIP Designer tool suite for automating and accelerating the design of application-specific instruction set processors (ASIPs)

Benefits

- Explored and optimized processor architecture to reduce area and system development cost
- Reduced gate count by 70% compared to fixed-function hardware accelerators
- Rapid architectural exploration using compiler-in-the-loop technology
- Automatic generation of a fully featured software development kit (SDK) including an optimizing C compiler
- No royalty costs

Overview

Fuji Xerox's full-color digital multifunction printer for office use incorporates the latest controller software to provide universal operability and software functions to help streamline customers' business operations. One of the key requirements of this new MFP was silent operation, to support quiet work environments. Angularity correction is typically done mechanically, but the need for quiet operation of office automation equipment required Fuji Xerox to take a different approach of using advanced image processing algorithms to apply the correction to the scanned image. This had to be implemented in a power-, performance- and area-efficient way, with the flexibility to make modifications to the algorithm. Fuji Xerox evaluated the implementation options, but none of the standard approaches met their requirements: a general-purpose processor would not deliver the required performance, and fixed-function hardware accelerators designed in RTL would result in a significant gate count increase. To meet their goals, Fuji Xerox decided on an application-specific instruction-set processor (ASIP) approach and selected Synopsys' ASIP Designer tool.

Efficient Application-Specific Processor Design

In contrast to standard fixed-function hardware accelerators, ASIPs enable the design of very efficient accelerators that are controlled by application-specific instructions rather than by a state machine. Due to its specialization, ASIPs can match the performance of fixed RTL designs and, by applying resource sharing, can result in smaller area. An ASIP is fully software programmable, so the algorithm can be changed even after tapeout.

Fuji Xerox selected Synopsys' ASIP Designer, the industry's leading ASIP design tool environment. ASIP Designer uses a single input specification to generate a software development kit (SDK) featuring a highly optimizing C compiler, instruction-set simulator (ISS), assembler, linker and debugger, as well as the synthesizable RTL. The generated ISS, including its advanced profiling capabilities, and the unique compiler-in-the-loop technology, allowed for rapid architectural exploration, as Fuji Xerox was able to profile the architecture against their algorithms right away. ASIP Designer's nML processor modeling language enabled the design team at Fuji Xerox to make rapid changes in the processor model, which were then reflected in RTL, C compiler, and simulator, making it easy to make iterative enhancements to the processor.

As predicted, the ASIP allowed significant resource sharing and enabled a 70% gate count reduction compared to individual fixed-function hardware accelerators. This made it possible for the design to fit into an FPGA, eliminating ASIC NRE costs.

Fuji Xerox completed their design, from concept to implementation, in just 14 months and with a limited team of two nML programmers, one person for tech support and one manager. With the successful conclusion of this project, the Fuji Xerox team is looking forward to continuing to use ASIP Designer.

"Synopsys' ASIP Designer provided us with the ability to start software development early and efficiently conduct architectural exploration and optimization of the design, saving a lot of time and freeing the development team to focus on other aspects of the project."

Noriaki Tsuchiya
Manager, Controller Development Group, Fuji Xerox

SYNOPSYS®
Silicon to Software™

Synopsys, Inc. • 690 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

09/15.rd.CS6505.