

Synopsys and DisplayLink

DisplayLink Achieves First-Pass Silicon Success with DesignWare SuperSpeed USB 3.0 IP



Synopsys delivered an IP solution that worked straight out of the box: the silicon came up and within hours very complicated data sets were streaming through high-speed interfaces. It's a testament to the quality of DesignWare IP that it functioned exactly as the spec said it would."



Jonathan Jeacocke
 Vice President of Engineering, DisplayLink

Business

DisplayLink is a semiconductor and software company that offers unique network display technology to enable easy virtual graphics connectivity between computers and displays over standard interfaces such as USB and Ethernet. Dozens of globally branded PC accessories including monitors, universal docking stations, display adapters, projectors and zero client systems that make expansion of the desktop visual workspace possible at significantly lower cost and energy usage than traditional solutions rely on DisplayLink chips.

Challenges

- ▶ Obtain high-quality IP that would enable first-pass silicon success
- ▶ Ensure device interoperability with industry standards through proven IP solutions
- ▶ Prototype, test and interoperate in a real-time environment to ensure "right first time" design

Synopsys Solutions

- ▶ DesignWare® SuperSpeed USB 3.0 Device and PHY
- ▶ DesignWare HDMI Transmitter Controller IP
- ▶ HAPS® FPGA-based Prototyping System

Benefits

- ▶ Achieved first-pass silicon success with DesignWare SuperSpeed USB 3.0 IP
- ▶ Reduced integration risk with compliant, certified DesignWare IP
- ▶ Validated system functionality at almost real-time speeds with HAPS FPGA-based prototypes

Overview

DisplayLink's highly integrated DL-3000 chip platform enables next-generation docking stations, displays and other integrated devices to move HD video and audio to multiple HD displays using SuperSpeed USB 3.0. It can simultaneously process beyond-HD video, Gigabit Ethernet and multi-channel audio. Video delivered from a standard USB 3.0 Host port enters the DL-3000 chipset through a USB 3.0 Device core and PHY and converts the data to HDMI or DVI for transmission to a TV or display. The DL-3100 chip delivers resolutions up to 2048 x 1152. Other DL-3000 chips can go to 2560 x 1600 pixels while enabling the use of dual HD monitors. Every chip in the DL-3000 family features DisplayLink's efficient adaptive compression technology, which dynamically

compresses video for transmission based on the content, available CPU cycles and USB bandwidth to deliver the best USB graphics experience at any given instant.

High-Quality DesignWare IP, Excellent Support

DisplayLink's DL-3000 chip platform takes advantage of USB 3.0 signaling speeds of up to 5 gigabits per second and enables peripherals to process multiple high-definition video signals. The DL-3000s can run up to two HD displays, networked data, high-resolution graphics and audio channels simultaneously through a single USB 3.0 controller and PHY. To develop the highly integrated, single-chip solution, DisplayLink needed reliable IP. Also, with the emerging USB 3.0 ecosystem, DisplayLink had to be certain that the IP selected would interoperate seamlessly with new USB 3.0 and existing USB 2.0 hosts. After using USB 2.0 IP from other vendors, DisplayLink switched to DesignWare IP including the USB 3.0 Device Controller, USB 3.0 PHY and HDMI Transmitter Controller. "When you buy standard IP blocks, you want to know the IP will do what you want it to do and that it will work straight out of the box," said Jonathan Jeacocke, vice president of Engineering, DisplayLink. "We selected Synopsys DesignWare IP because we were extremely confident that the IP would do exactly what it was supposed to do, and it did." With IP composing a large portion of their design, the DisplayLink design team didn't want to assume the risks associating with porting all the IP to their foundry process of choice. Knowing that Synopsys' DesignWare PHY IP was silicon-proven on DisplayLink's required foundry process made the decision to use Synopsys an easy one.

When DisplayLink started their USB 3.0 design, the USB 3.0 specification was new and still evolving so it was important to them to work with an IP vendor that was actively involved in the standard. Additionally, DisplayLink worked closely with Synopsys and provided valuable feedback on IP usage that led to a more optimized implementation. "The endpoint optimizations improved memory utilization in our design and enabled us to meet our performance requirements," said Jeacocke.

Leading Hardware Prototyping System

To reduce the design risk inherent in implementing an evolving standard, DisplayLink used Synopsys' HAPS FPGA-based Prototyping System to validate the functionality of their design and to develop software in parallel with the ASIC development. On a large SoC it is critical to ensure communication between analog PHYs and digital logic. By using the HAPS USB 3.0 PHY daughter card, the DisplayLink design team was able to validate the working system at almost real-time speeds, months ahead of silicon availability, and debug software well before tape out. They had the added benefit of being able to demonstrate the end product to customers long before silicon came back. "It's an incredible value proposition to be able to not just tell our lead customers that the design will work, but to demonstrate it on a prototyping platform for them to see with their own eyes," said Jonathan Jeacocke, vice president of Engineering, DisplayLink. "By using HAPS, we had absolute confidence that the final silicon design would work the very first time."

With this success behind them, DisplayLink has started a follow-on design using additional Synopsys IP and HAPS systems.

"We asked Synopsys for some endpoint optimizations, which enabled us to improve memory utilization and meet performance requirements. Synopsys support was very good — the support team was extremely responsive throughout our design process."

Jonathan Jeacocke

Vice President of Engineering, DisplayLink

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