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Synopsys and Cognitive Systems Corp.

Cognitive Systems Achieves First-Pass Silicon Success for Multi-Core Cognitive Radio Chip Using ASIP Designer

COGNITIVE∞

"Cognitive Systems Corp. built Aura, a thoughtful security solution for the home, which required advanced signal processing capabilities while being able to achieve superior processing performance with high energy efficiency. Application-optimized processors are a key requirement to obtain this goal and by using Synopsys' ASIP Designer, Cognitive Systems was able to design two different custom processors within 12 months and with a small team."—- *Oleksiy Kravets, Chief Technology Officer, Cognitive Systems Corp.*

Business

Cognitive Systems Corp., headquartered in Waterloo, ON, Canada, provides a solution for home monitoring using radio signals and wireless spectrum analytics. Aura is an easy to install, two-sensor system that allows people to understand motion in their home, without the use of cameras, by analyzing the disruption of wireless signals using patented technology by Cognitive Systems. The ability to sense wireless activity and, as a result, perform actions opens up new business opportunities leveraging wireless devices and infrastructure that are already in place. Cognitive provides a complete solution, including the aggregation and processing of data from the sensors or a network of sensors, and enabling cloud-to-cloud connection. Using a secure API, the Cognitive platform allows for easy and rapid integration into security platforms.

Challenges

- Design a chipset that allows for spectrum analysis of a wide spectrum between 650 MHz and 4 GHz, supporting a large variety of wireless standards
- Optimize for power efficiency and performance, to allow for mobile deployments
- Develop within less than 12 months, with a small team

Synopsys Solution

- ASIP Designer

Benefits

- Developed a fully programmable digital signal processing solution that allows for easy adaptation to multiple wireless standards
- Explored and optimized two different processors for a multi-core processor architecture to meet performance requirements, using ASIP Designer's compiler-in-the-loop technology

- Massive parallel processing of wireless signals using a highly specialized, yet fully C-programmable, combined SIMD/VLIW processor architecture offering up to 46 GOPS at 312 MHz, using 40-nm LP technology
- 32-bit dual-core MCU for system control and real-time task scheduling
- Full-featured software development kit (SDK) including an optimizing C-compiler
- No royalty costs

Overview

At the heart of Cognitive Systems' solutions is a proprietary cognitive radio that can cover spectrums between 650 MHz and 4 GHz. The cognitive radio chipset provides a wideband view of the wireless signals, which enables spectrum data to be extracted and processed. The chipset includes four RF receiver paths, RF transmitter, eight DSP datapaths, a dual-core vector processor with dedicated vector memory, dual-core microprocessor, forward error correction (FEC), and a linear RF front-end system.

Cognitive Systems needed to implement the entire solution, from concept to silicon, in less than 12 months, with a small engineering team. Being a venture-capital funded startup, first silicon success was essential.

Cognitive Systems realized the need for a fully programmable solution to keep the solution flexible enough for different markets, regions and use cases. The system architecture called for a first processor to handle control-dominated functionality including hard real-time scheduling tasks. A second processor, tailored to vector-based signal processing capabilities required to demodulate, sense, and analyze the IQ signals coming from the multiple receiver paths, was also needed. The system requirements called for extremely high performance for the proprietary spectrum sensing algorithms along with low power consumption, as is normally required for compact mobile devices.

Starting from the application-specific signal processing requirements, Cognitive analyzed available DSP processor IP. They quickly recognized that no processor IP available on the market would provide both the required data throughput, and the performance/mW required for the signal processing functionality. As a result they decided to develop their own, highly specialized vector processor – an application-specific instruction set processor (ASIP).

The specialists at Cognitive had prior experience with designing processors. It was obvious to them that they had to use a powerful tool solution that would allow them to develop a processor within the very limited time budget and with the small team at hand. They turned to Synopsys' ASIP Designer tool solution.

ASIP Designer

ASIP Designer is the industry's leading ASIP design tool environment, accelerating the design, verification and programming of customer-designed processors. ASIP Designer uses a single input specification (nML) to generate a software development kit (SDK) featuring a highly optimizing C/C++ compiler, cycle- and instruction-accurate instruction-set simulator (ISS), assembler, linker and debugger, as well as the synthesizable RTL. The generated ISS, including its advanced profiling capabilities, and the unique compiler-in-the-loop technology, allow for rapid architectural exploration, as users can profile the architecture against their algorithms right away. ASIP Designer comes with a large number of example models written in nML and provided in source code, which serve both as a reference, as well as a starting point for customer-specific designs.

The Development Process

Given the short development cycle, the engineers at Cognitive had to establish a very efficient design process, with the ability to execute multiple distinct design activities in parallel while also iterating quickly on design changes. Two elements were especially crucial: early involvement of the embedded software developers to get feedback on the proposed architecture, and a rapid path to an FPGA prototype for design validation. Using ASIP Designer, Cognitive architects quickly came up with a first processor architecture described in nML. The automatically adapted C/C++ compiler enabled software engineers to profile the architecture using the algorithms being developed for the final product, providing early feedback on all aspects of the architecture, ranging from the memory and register configuration to the pipeline structure and the instruction set definition. Using the RTL generation capability, moving to an FPGA-based prototype

was also possible very early in the design process. This enabled the prototyping environment to be set up while the architecture design was still ongoing. The architects then used feedback from both the software engineers and the prototyping experience to incrementally optimize and refine the nML description of the architecture, automatically keeping the software tools and prototype in sync throughout the design process.

For the control processor, Cognitive utilized one of the example models provided with ASIP Designer, as the starting point. Starting from a fully-functional 32-bit RISC architecture written in nML with complete compiler support, Cognitive was able to rapidly tune the processor architecture to the real application code being developed by the software team.

The Result

In under a year, Cognitive designed a dual-core SIMD/VLIW vector processor and a companion control processor. The I/Q data vector is 256-bits wide, storing eight I/Q samples. Each core of the vector processor has a 348-bit instruction that encodes 12 opcodes, which allows for up to 150 word operations (including load/store) per clock cycle at 312 MHz – resulting in up to 46 GOPS, and processing of up to 54 IQ samples per clock-cycle. Vector ALUs with DSP capability balance performance, area, and power. A mix of vector and scalar operations offer a flexible combination of fully vectored / parallel execution for signal processing, and sequential "MCU-like" execution suitable for control.

A 32-bit dual-core MCU runs embedded applications and provides system control and real-time task scheduling/coordination. Each MCU has a three-stage execution pipeline, Harvard memory architecture, and tightly coupled (parallel access, single-cycle latency) data and instruction memory. The design was done in a 40-nm LP process.

Both processors are fully C-programmable, leveraging ASIP Designer's unique compiler generation capability.

The entire mixed-signal radio design including the processor development was completed in less than one year, from algorithm to first silicon, including FPGA-based prototyping. The team included two processor architects, up to five people involved in hardware design, and five embedded software developers.

ASIPs and ASIP Designer are central to Cognitive's products' capabilities and differentiation, and their ability to develop their solution with an eye toward fast time-to-market and a minimum of engineering resources. Having achieved first-pass silicon success, Cognitive is pleased with the benefits they realized with ASIP Designer and expect to use it for future projects with similar requirements.

> *"Synopsys' ASIP Designer provides a fully-functional software development kit at any stage of the design process, which allowed us to take an iterative design approach with processor designers and embedded software developers working close cooperation. This capability was fundamental to enabling us to meet our project timelines."* —- *Oleksiy Kravets, Chief Technology Officer, Cognitive Systems Corp.*

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