SYNOPSYS®

MIPI D-PHY Gen3 TX Integration Review Checklist

Application Note

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Revision History

Date	Description
December 2018	Updated: ■ Reference Documents ■ Integration Checkpoints
June 2016	Updated: ■ Table 2-2 Synthesis Checklist
February 2015	Document created

Reference Documents

The documents listed below, included in the IP product package, are referenced throughout this Application Note:

- Databook, found under: “doc/<product_name>_databook.pdf”;
- Release Notes, found under: “doc/readme_[revision].txt”;
- Verilog Quickstart Testbench, found under: “macro/testbench/<product_name>_qst.v”.

1 Introduction

1.1 Scope

The purpose of this Application Note is to list the items known to be fundamental for successful IP integration. A checklist must be concise, by designing a best practice and a meticulous review which applies all the recommendations in the databook for proper IP integration and operations.

This Application Note is actively maintained; please ensure you have the latest version of this document.

Download the latest version of this Application Note from the documentation section of the IP Directory under http://www.mydesignware.com.

At any point, your Applications Engineering (AE) Support team is available for clarifications and support through the SolvNet platform.

1.2 Integration Review Services

Integration Review Services are part of the Synopsys Standard Core Support. AE engineers perform visual inspection of your implementation to identify common pitfalls. For these reasons it is highly recommended to include the Review Services in your planning.

Synopsys recommends reviews at the completion of each stage:

- Logical Integration and Testability;
- Synthesis;
- STA and Post Layout Simulation;
- GDS Layout;
- Package Design;
- PCB Design.

1.3 Instructions

This Application Note includes Checklist Tables organized by Integration Stage.

The answer to all items is expected to be “Yes”. Promptly contact the Synopsys Support Team if any item is foreseen to not be fulfilled.

Depending on the Integration Stage review the applicable table and:

1. Carefully review the item “Description”;
2. Explore the “Reference Materials” for further details;
3. Answer “Yes” or “No” to the questions;
4. Add relevant comments;
5. Provide the filled in Checklist to Synopsys.

2 Integration Checkpoints

2.1 Logical Integration and Testability Review

Access to PPI controllable and observable signals is strongly recommended for complete debugging capabilities.

Table 2-1 Logical Integration and Testability Checklist

	Description	Yes/No	Comments	Reference Materials
L1	Review the Instantiation in the Verilog wrapper: 1. Are the IP hard and soft macro instantiated? 2. Is the PLL macro instantiated?			Standard Deliverables, Wrapper example
L2	Review digital interface of the IP: 1. (Does the pin connection follows “Signal Descriptions” as described in the Databook? 2. Are all inputs connected? 3. Is IP input signal txbyteclkhs connected to txbyteclksrc IP output signal? 4. Are the Controllable and Observable signals not tied to 1 or 0, nor left unconnected? 5. Have you ensured that scanluctrl default value (1’b1) is NOT changed to 1’b0? 6. In case the PLL SoC interface is not used: Is shadow_clear signal is accessible? (a pulse should be given on shadow_clear signal to avoid a X simulation artifact)			Databook, “Signal Descriptions” section Databook, “Gate level System Verification”

Table 2-1 Logical Integration and Testability Checklist (Continued)

	Description	Yes/No	Comments	Reference Materials
L3	1. Are the following clock signals and frequencies within the range defined in the databook? - FREFCLK - FCFG_CLK - TXCLKESC - TESTCLK - SCAN_<clock_domain>_in (if applicable) 2. Does the jitter of REFCLK meet the requirement described in the databook?			Databook, “Functional Description” and “Process-Specific Specifications” sections
L4	Review the DPHY configuration: 1. Is the DPHY configured through TestCode in SHUTDOWN mode? 2. Is the cfgclkfreqrange[7:0] configured according to FCFG_CLK? 3. Is the hsfreqrange[6:0] signal or register – Testcode: 0x01 and 0x02 – configured for the operating bit rate? 4. Is the slew rate configuration performed as part of the IP start-up?			Databook, “Functional Description” section
L5	Review the PLL configuration: 1. Are the PLL parameters configured through TestCode or SoC for the expected operating bit rate while IP is in shutdown mode?			Databook, “PLL Modes of Operation” section

Table 2-1 Logical Integration and Testability Checklist (Continued)

	Description	Yes/No	Comments	Reference Materials
L6	Review testbench and simulation waveform: 1. Is the simulation timescale set as the delivered testbench? 2. Are all input signals set to high or low logic level? 3. Is the Startup-up sequence followed? 4. Is the correct I/O driver strength used in Testbench? (For LP use command: bufif1 (pull0,pull1) #(TRISE,TFALL) (OUT, IN, ENABLE); For HS use command:bufif1 (supply0,supply1) #(TRISE,TFALL) (OUT, IN, ENABLE);) 5. Are all the input stimuli and register configuration according to databook description? 6. Are all the operating modes and production tests simulated? 7. Is scanclk or scan_<clock_domain>_in (if applicable) not toggling when IP is not in Scan Mode?			Standard Deliverables, Quickstart Testbench Databook, “Functional Description” and “Functional Verification” sections
L7	Are isolation cells added at IP output signals when IP digital supply is turned off (floating) and the block that it is interfacing with has the logic domain always ON?			
L8	Are the test interface signals controllable and observable?			Databook, “Control and Test Modes” section
L9	Are all the signals required to implement Characterization and Production Test plan controllable and observable?			Databook, “Characterization and Production Tests” section
L10	In case of REXT sharing between multiple DPHYs: Is the power up of the DPHYs is done sequentially? (one after one)			Databook, “External Reference Resistor”

2.2 Synthesis Review

Table 2-2 Synthesis Checklist

	Description	Yes/No	Comments	Reference Materials
S1	Review Synthesis in log file: 1. In the Design Compliler: - Is the variable “hdlin_keep_signal_name” set to “user”? - Is the variable “dont_touch_nets_with_size_only_cells ” set to “true”? 2. Is the timing constraint file of the deliverable referenced when doing synthesis? 3. Are the boundary and input/output delay constraints in constraint file of deliverable removed when IP is synthesized together with controller? 4. Is there any Error in synthesis log? 5. Is there any timing violation in synthesis log? Are there any FFs without clock? Use command: check_timing -verbose			Databook, “Synthesis” section

2.3 STA and Post Layout Simulation Review

Table 2-3 STA and Post Layout Simulation Checklist

	Description	Yes/No	Comments	Reference Materials
T1	Is STA performed with the IP timing library (.lib/.db) and the intended operation mode specified with the set_mode command?			Databook, “Clock Timing Model” and “Static Timing Analysis” sections
T2	Are all required clocks and generated clocks defined for each mode of operation and set_propagated_clock [all_clocks] command used? 1. Are no unconstrained paths? Use command: check_timing -verbose			Databook, “Clock Timing Model” section
T3	Are any additional cells (example ESD clamps, isolation cells, …) accounted for timing?			STA Flow
T4	Is timing closed for best and worst case corners (at least) and timing violations clean?			STA Flow
T5	Review Post layout simulation: 1. Is the .sdf file (located in the “macro/timing/sdf” folder) used for post layout simulation? 2. Does the gate level simulation run for extreme corners (example best and worst case)?			Databook, " Clock Timing Model " and “Gate level System Verification” sections
T6	Review SCAN simulation: 1. Has stuck-at and ASST (if applicable) been simulated with the IP using ATPG patterns generated after SoC integration? 2. Is the behavior model (gate level and sdf) used for ATPG simulation? (ATPG model is only used for pattern generation, not for ATPG simulation)			Standard Deliverables, atpg, “testbench” and “sim” folders Databook, “Scan Mode” section

2.4 GDS Layout Review

Table 2-4 GDS Layout Checklist

	Description	Yes/No	Comments	Reference Materials
G1	1. Is the D-PHY orientation and integration allowed for single or multiple instances? 2. Is VDD and VSS Power Domain integration scheme SoC or IP oriented based?			Databook, “Physical- Level Implementation” section
G2	Review the Floorplan: 1. Is the IP placed away from any noisy circuitry? If not, is an extra 10 µm N-well moat tied to vph added? 2. Is the IP located on the die periphery of the ASIC? 3. Are there any devices within the region from IP boundary as described in the databook? 4. Are the I/O connection add-on blocks connected to IP macro by abutment? 5. Is the PLL connected to IP macro and I/O connection add-on block by abutment? 6. Are the integrated blocks integrated with the defined offset position? 7. Is the IP correctly orientated in the SoC?			Databook, “Physical- Level Implementation” section
G3	Review the Routing: 1. Is there no routing over its area, in any layer except IP related RDL and bumps? 2. Is there no unrelated routing within the region from IP boundary as described in the databook? 3. Is the routing to the IP pins done orthogonally? 4. Are all the metal layers connected at the location of the defined pin? 5. Is the connection width at least the same as pin width? 6. Are the foundry electromigration guidelines applied?			Databook, “Physical- Level Implementation” section

Table 2-4 GDS Layout Checklist (Continued)

	Description	Yes/No	Comments	Reference Materials
G4	Review the Digital Power connection: 1. Are all the IP digital power pins connected to the SOC digital power with the specified pin metal layers and pin width? 2. Are all the PLL power pins connected to the SOC digital power mesh with the specified pin metal layers and pin width? 3. Is the voltage drop including power mesh, RDL, package and PCB routing taken into account? 4. Is the maximum ripple noise (peak-peak) amplitude less than the value defined in the databook?			Databook, “Physical- Level Implementation” section
G5	Review I/O add-on connection block: 1. Is the I/O add-on connection block used without any changes? 2. Are the proper I/O block instantiated for the integration? - pads_* for IP without PLL - pads_*_pll for IP with PLL			Databook, “Physical- Level Implementation” section
G6	Review the Analog Power connection (if I/O add-on blocks not used): 1. Is the resistance of RDL routing for vph/vp/gd less than the value defined in the databook? 2. Is the PLL analog supply (vpl) shorted with vp pin (resistance below the databook guideline) 3. Is the maximum ripple noise (peak-peak) amplitude less than the value defined in the databook?			Databook, “Physical- Level Implementation” section
G7	Review the Diff pairs connection (if I/O add- on blocks not used): 1. Are complementary *P and *N routings symmetrical and resistance and capacitance balanced including RDL routing, bonding wires and PCB traces? 2. Are the resistance and capacitance of RDL routings for *P and *N less than the value as described in the databook? 3. Are the R and C mismatch of *P and *N RDL routing less than 10%?			Databook, “Physical- Level Implementation” section

Table 2-4 GDS Layout Checklist (Continued)

	Description	Yes/No	Comments	Reference Materials
G8	Review Analog Auxiliary Signals – atb/rext (if I/O add-on blocks not used): 1. Is the resistance and capacitance of RDL routings for rext signal less than the value defined in the databook? 2. Is the resistance and capacitance of RDL routings for atb signal less than the value defined in the databook?			Databook, “Physical- Level Implementation” section
G9	Review the ESD ring, if using I/O add-on blocks: 1. Are vss and vdd power clamps placed at a maximum distance of 200um spacing from the PHY boundary? 2. Is the maximum vdd/vss routing resistance from SoC power clamps to PHY boundary border less value defined in the databook?			Databook, “Physical- Level Implementation” section
G10	Dummy Filling Is the filling strategy being applied?			Foundry DRC Rules
G11	Review the LVS/DRC: 1. Is the LVS/DRC sign off deck the same the SNPS sign off deck? 2. Are the LVS/DRC switch settings as per SNPS recommendations? 3. Is IP LVS/DRC passed at chip-level? 4. If there are no new DRC errors inside the IP hard macro boundary? 5. Is the latest released GDS integrated and not modified? Perform XOR comparison between SoC GDS to latest IP GDS release.			readme file
G12	External Reference Resistor (rext) shared (if applicable) 1. Is there only one IP using the external Reference resistor (forcing current across the resistor) at the same time? 2. Shared is done based on guidelines: i. Sharing a BGA ball ii. Sharing a single bump 3. Is the total capacitance on rext pad lower than the value defined in the databook?			Databook, “External Reference Resistor” section

2.5 Package Design Review

Table 2-5 Package Design Checklist

	Description	Yes/No	Comments	Reference Materials
P1	Are the analog power supply domains separated?			Databook, “Physical- Level Implementation” section
P2	Are all the analog power and ground pads of IP connected to the package pins?			Databook, “Physical- Level Implementation” section
P3	Are all the SoC and IP grounds shorted? Note: The number of package balls needed should be estimated based on switching activity, current consumption and signal integrity requirements.			Databook, “Physical- Level Implementation” section
P4	Are package differential insertion losses within recommended values?			Databook, “Board- and Package-Level Implementation” section
P5	Is the maximum ripple noise (peak-peak) amplitude less than the value defined in the databook?			Databook, “Physical- Level Implementation” section
P6	Are all the differential pairs signals routed with matching lengths, and 100 ohm differential characteristic impedance?			Databook, “Board- and Package-Level Implementation” section
P7	Are power and signal integrity simulations done with real package, and estimated board model?			Standard Deliverables, “hspice” delivered folder

2.6 PCB Design Review

Table 2-6 PCB Design Checklist

	Description	Yes/No	Comments	Reference Materials
B1	External Reference Resistor: 1. Is the 1% tolerance (E96 series external termination resistor placed on REXT pin for calibration? 2. Is the external resistor shared between multiple PHYs and not used by each IP at same time? 3. Is the total capacitance on rext pad lower than the value defined in the databook?			Databook, “Physical- Level Implementation “and PCB Guidelines” sections
B2	Are power decoupling capacitors of appropriate value added near the power supply pins? Note: Capacitors of smaller value should be placed closer to pin.			Databook, “PCB Guidelines” section
B3	Is each IP power supply connection isolated through an inductive choke?			
B4	Are the power supplies within reference values?			Databook, “PCB Guidelines” section
B5	Is the maximum ripple noise (peak-peak) amplitude less than the value defined in the databook?			Databook, " Physical- Level Implementation " section
B6	Are all the differential pairs signals routed with matching lengths, and 100 ohm differential characteristic impedance?			Databook, “PCB Guidelines” section
B7	Are power and signal integrity simulations done with real board and package model?			Standard Deliverables, “hspice” folder