SYNOPSYS®

USB 3.1/DP Alt PHY INTEGRATION REVIEW CHECKLIST
Application Note

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Contents

Revision History

Doc. Revision	Date	Description
1.0	2016/11/08	Initial revision

Reference Documents

The following reference documents are used in this application note:

- *IP Databook*, IP product package under "doc"
- *Read Me*, IP Product package under "doc/readme_[rel_version].txt
- *DesignWare Cores Consumer 10 USB 3.1 SS+ PHY ATE Test Bench*, IP product package under "doc"
- *USB 3.1 SS Plus PCS for the DesignWare Cores USB 3.1 SS Plus PHY*, IP product package under "doc"
- USB 3.1 specification, available from http://www.usb.org/developers/docs/
- VESA DisplayPort Alt Mode on USB Type-C Standard from http://www.vesa.org/
- VESA DisplayPort (DP) Standard from http://www.vesa.org/

1 Introduction

1.1 Scope

This Application Note lists important Checkpoints to be verified at different Integration stages, such that typical pitfalls during the Integration of Synopsys IP can be mitigated.

Not all the IP Integration requirements are listed exhaustively in this document, therefore general design best practices and carefully reviewing/following the IP databook is necessary to ensure proper Integration and Operation of Synopsys IP.

This Application Note is actively maintained; therefore it is important to use the latest version of this document.

Note	Download the latest version of this Application Note from the documentation section of the IP Directory under www.mydesignware.com

For clarifications or Integration Support, your Corporate Applications Engineering Support team can be reached through SolvNet.

1.2 Integration Review Services

In this context it is also important to highlight that Synopsys provides Integration Review Services as part of the Standard Core Support.

The Integration Review Services consist in visual implementation reviews, carried out by Synopsys Corporate Applications Engineers, focused on helping the customer improve the odds of SoC success.

Synopsys recommends customers to include time for the Reviews on their planning as they typically allow early detection of the most typical customer pitfalls.

The following reviews are included as part of this Service:

- Logical Integration Review;
- Post P&R Static Timing Review;
- GDS Layout Review;
- Package Review;
- PCB Review.

1.3 Instructions

For your convenience, this Application Note includes Checklist Tables organized by Integration State. Depending on the Integration State, review the applicable table and:

1. Carefully review the “Description” column;
2. For clarifications, the “Reference Materials” column points out the relevant documentation;
3. Type Yes or No in the “Yes/No” column. For correct Integration answers in this column are expected to be marked as “Yes”;
4. Add any relevant clarifications to the “Comments” section;
5. Submit the filled Checklist to Synopsys as part of the Integration Review.

2 Logical Integration Review

2.1 Logical Integration Review Checkpoints

Table 2-1 Logical Integration Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
L1	Review Clock source settings, (a) Is ref_use_pad set for your reference clock input choice?			IP Databook, "Signal Descriptions" section
L2	Review Clock frequency settings, (a) Are the Support block input signals set to the proper settings for your reference clock frequency?			IP Databook, “Configuring for USB 3.1 SS+” section
L3	Review reference clock input signal, (a) Are the requirements (duty cycle, jitter, etc.) for the reference clock met?			IP Databook, “Reference Clock Requirements" section
L4	Review Tune bit signal connections, (a) Are the parameter control signals (protocol[0,1,2]_ext*) controllable? (b) Is the phy_ext_ctrl_sel controllable? Note: protocol1_ext_* signals are only used in USB 3.1 mode as pcs_laneX_protocol[1:0] should be set to 2’b01 for USB 3.1. (c) Are the dp_txY_* and dp_mpllb_* signals controllable? Note: These signals are only used in DP Alt mode.			(a) PCS Databook “Miscellaneous Interface Signals (PHY Configuration)” (b) IP Databook, "Lane Settings for USB 3.1 SS+" section (c) IP Databook, "TX Equalization and Adaptation" section (d) IP Databook “RX Equalization” (e) IP Databook, "Boundary Scan (ACJTAG)" section

	Description	Yes/No	Comments	Reference Materials
L5	Review signal pin connections, (a) Are the test pins de-asserted for normal operation? (b) Are all reserved signals driven to the appropriate value (e.g. dp_txY_flyover_data_{p,m})? (c) If using boundary scan, are the signals set correctly?			IP Databook, "Signal Descriptions" section
L6	Review testbench and simulation, (a) Has the phy model been integrated and passed? (b) Has a simulation been run without ANI_SHORT_RESET macro defined and without the FAST_FLAG registers set? (c) Are all inputs driven to non "X", including JTAG. (d) Is your simulation timescale set to 1ns/10fs?			IP Databook, "Simulation Environment" section IP Databook, " Fast Simulation Mode" section
L7	Are the voltage levels of power supplies within the reference values?			IP Databook, "Power and Ground" section
L8	Reference Clock Pin connections: (a) Ensure *ONLY* one differential pair of clock pins, either from PAD (REFPADCLK{M|P}) or SoC (REFALTCLK{M|P}), can be activated at the same time (b) Ensure the non-used pair of reference clock inputs must be held at static state or stays grounded on board/chip			N/A
L9	Ensure there is no inadvertently floating PHY input on ASIC side			N/A
L10	Is the PHY being used in a comboPHY configuration (USB 3.1 and DP Alt mode)? (a) Are the TCA signals being controlled correctly? (b) Is the TCA APB interface accessible?			IP Databook “DPAlt Crossbar and TCA” section

	Description	Yes/No	Comments	Reference Materials
L11	Is power gating being enabled for the PHY? (a) Is the pma_pwr_en output signal from the PHY connected externally to the ana_pwr_en input of the PHY? (b) Is the ana_pwr_stable output signal from the PHY connected externally to the pma_pwr_stable input of the PHY? Note: If power gating is disabled, the *_pwr_en and *_pwr_stable input signals, respectively, should be tied to 1'b1.			IP Databook "Power Gating" section

3 Post P&R Static Timing Review

3.1 Post P&R Static Timing Review Checkpoints

Table 3-1 Post P&R Static Timing Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
T1	Is STA performed with the IP timing lib .lib/.db and the intended operation mode specified with the set_mode command?			IP Databook, " PMA PCS Synthesis" section
T2	Are all the required clocks and generated clocks for each mode of operation defined as per the synthesis constraints?			IP Databook, " PMA PCS Synthesis" section
T3	Has the txX_clk path been analyzed across VT corners to ensure that the path delay variation is within the external txX_clk margin requirements?			IP Databook, "txX_clk constraints" section
T4	Are SDF timings for the rest of the SoC (i.e., other than the IP) derived from extracted parasitics?			STA Flow
T5	Is timing closed for best and worst case corners (at least) and setup/hold violations are clean?			STA Flow
T6	Are gate level simulations performed for both best and worst case corners?			IP Databook, "Verilog Model Files and Simulators" section

4 GDS Review

4.1 GDS Review Checkpoints

Table 4-1 GDS Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
G1	Is the latest released GDS integrated and not modified? Suggest to compare SoC GDS to latest release IP GDS.			Standard Deliverables, GDS file
G2	Are the layers above the IP properly filled? The foundry dummy fill generation utility should be used and DRC should be confirmed to be clean post-fill.			Foundry DRC Rules, Standard Deliverables, Readme file
G3	Is the IP correctly orientated in the SoC?			Foundry DRC Rules
G4	Is the IP placed close to die corner? (a) It is recommended to place the macro at the center of the side of the die.			IP Databook, “Physical-Level Implementation" section
G5	Is there is a keep-out area around the macro boundary? (a) No unrelated routings or devices within 10 µm.			IP Databook, “Physical Implementation Guidelines" section
G6	Are vsscore pins of the PHY connected to the SoC vsscore supply grid and is the extracted connection resistance below the recommended value?			IP Databook, " ESD Back-to-Back Diode Connection to Core VSS" section
G7	Check "cell integrity", (a) No RDL routing from other IPs within the IP area? (b) No routing on top of IP (except RDL routing of IP)?			N/A

	Description	Yes/No	Comments	Reference Materials
G8	Does routing to IP pins follow these guidelines? (a) Orthogonal to the macro boundary; (b) All the metal layers where the pin is defined are connected (excluding PHY macro side power/ground signals); (c) Connection width is at least same as pin width.			N/A
G9	Is the LVS/DRC sign off deck same as or newer than the SNPS sign off deck?			Standard Deliverables, Readme file
G10	Are the LVS/DRC switch settings as per SNPS recommendations?			Standard Deliverables, Readme file
G11	Does chip-level LVS/DRC pass with the PHY?			Standard Deliverables, Readme file

5 Package Review

5.1 Package Review Checkpoints

Table 5-1 Package Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
P1	Power/Ground Connections (a) Are the vph and vptxX/vpdig/vp pins, respectively, isolated on die? (b) Are the grounds common?			IP Databook, “Power Supply Sharing" section
P2	Are extracted RLC parasitics within recommended values?			IP Databook, "Board and Package-Level Implementation" section
P3	Are the txX_p/tx_X_m and txrxX_p/txrxX_m signal differential pairs routed with matching lengths and 100 Ω differential characteristic impedance, respectively?			IP Databook, "Signal Package and Board Guidelines" section
P4	Are the txX_p/tx_X_m and txrxX_p/txrxX_m signal differential lines matched in order to avoid data skew issues?			VESA DisplayPort Alt Mode on USB Type-C Standard (Section 4.2.3.1)
P5	Are the power supplies voltages within the reference value?			IP Databook, "Power and Ground" section
P6	Are power and signal integrity simulations results according to recommendations? (a) Package and PHY signal path comply with DisplayPort Standard; (b) Power supply ripple noise at IP pins is < 3% (peak to peak) and < 5% for vph and vp/vptxX/vpdig, respectively, at all frequencies.			General PHY recommendatons IP Databook, "Power Supplies Delivery to Pads" section

6 PCB Review

6.1 PCB Review Checkpoints

Table 6-1 PCB Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
B1	Is the 1% tolerance reference resistor of the specified value placed for resref pin?			IP Databook, “Reference Resistor Requirements" section
B2	Are power decoupling capacitors of appropriate value added near the power supply pins? Note that capacitors of smaller value should be placed closer to pin.			IP Databook “Board Bypass Capacitors” section
B3	Are the signal txX_p/tx_X_m and txrxX_p/txrxX_m signal differential pairs routed with matching lengths and 100 Ω differential characteristic impedance?			IP Databook “Board-Specific Routing Guidelines” section
B4	Are the txX_p/tx_X_m and txrxX_p/txrxX_m signal differential lines matched in order to avoid data skew issues?			VESA DisplayPort Alt Mode on USB Type-C Standard (Section 4.2.3.1)
B5	Are the power supply voltages within the reference value?			IP Databook, "Power and Ground" section
B6	Are power and signal integrity simulations results according to recommendations? (a) Package and PHY signal path comply with DisplayPort Standard; (b) Power supply ripple noise at IP pins is < 3% (peak to peak) and < 5% for vph and vp/vptxX/vpdig, respectively, at all frequencies			General PHY recommendatons IP Databook, “Power Supplies Delivery to Pads" section

7 Testability

7.1 Testability Checkpoints

Note	Access to controllable and observable signals is strongly recommended for complete debugging capabilities.

Table 7-1 Testability Checkpoints

	Description	Yes/No	Comments	Reference Materials
TS1	Are the control register signals and/or JTAG pins controllable and observable for debugging and testing purposes?			IP Databook, “Control Register Interface” section
TS2	Is the external SRAM interface used?			IP Databook, “External SRAM Support” section
TS3	Are the analog test bus (ATB) and digital test bus (DTB) used accessing internal voltages and digital signals, respectively, for debug purposes?			IP Databook “ATB and DTB Signals” section