SYNOPSYS®

DP AUX/AUX-I2C PHY INTEGRATION REVIEW CHECKLIST
Application Note

Version 1.0
February 2017

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Contents

Revision History

Doc. Revision	Date	Description
1.0	2017/02/21	Initial revision

Reference Documents

The following reference documents are used in this application note:

- *IP Databook*, IP product package under "doc"
- *Read Me*, IP Product package under "doc/readme_[rel_version].txt"
- *DP AUX PHY for the DesignWare Cores DP AUX PHY*, IP product package under "doc" or
- *DP AUX-I2C PHY for the DesignWare Cores DP AUX-I2C PHY*, IP product package under "doc"
- USB 3.1 specification, available from http://www.usb.org/developers/docs/
- VESA DisplayPort Alt Mode on USB Type-C Standard from http://www.vesa.org/
- VESA DisplayPort (DP) Standard from http://www.vesa.org/

1 Introduction

1.1 Scope

This Application Note lists important Checkpoints to be verified at different Integration stages, such that typical pitfalls during the Integration of Synopsys IP can be mitigated.

Not all the IP Integration requirements are listed exhaustively in this document, therefore general design best practices and carefully reviewing/following the IP databook is necessary to ensure proper Integration and Operation of Synopsys IP.

This Application Note is actively maintained; therefore, it is important to use the latest version of this document.

Note	Download the latest version of this Application Note from the documentation section of the IP Directory under www.mydesignware.com

For clarifications or Integration Support, your Corporate Applications Engineering Support team can be reached through SolvNet.

1.2 Integration Review Services

In this context, it is also important to highlight that Synopsys provides Integration Review Services as part of the Standard Core Support.

The Integration Review Services consist in visual implementation reviews, carried out by Synopsys Corporate Applications Engineers, focused on helping the customer improve the odds of SoC success.

Synopsys recommends customers to include time for the Reviews on their planning as they typically allow early detection of the most typical customer pitfalls.

The following reviews are included as part of this Service:

- Logical Integration Review;
- Post P&R Static Timing Review;
- GDS Layout Review;
- Package Review;
- PCB Review.

1.3 Instructions

For your convenience, this Application Note includes Checklist Tables organized by Integration State. Depending on the Integration State, review the applicable table and:

1. Carefully review the “Description” column;
2. For clarifications, the “Reference Materials” column points out the relevant documentation;
3. Type Yes or No in the “Yes/No” column. For correct Integration answers in this column are expected to be marked as “Yes”;
4. Add any relevant clarifications to the “Comments” section;
5. Submit the filled Checklist to Synopsys as part of the Integration Review.

2 Logical Integration Review

2.1 Logical Integration Review Checkpoints

Table 2-1 Logical Integration Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
L1	Review Tune bit signal connections, (a) Are the parameter control signals (AUX_*_TUNE) controllable? (b) For PHYs that support I2C, are the parameter control signals (I2C_*_TUNE) controllable?			(a) IP Databook, “AUX Tune Signals” section (b) IP Databook, "I2C Pins” section
L2	Review signal pin connections, (a) Are the test pins de-asserted for normal operation (e.g. AUX_CTRL[3])?			IP Databook, "Signal Descriptions" section
L3	Review AUX I2C Common Pins (a) For PHYs supporting dual modes (AUX and I2C), is AUXMODE and I2CMODE signals being driven correctly?			IP Databook, “AUX and I2C Common Pins” section
L4	Review I2C Signals For PHYs that supports I2C, is the I2C_VPH_1V2_EN signal set correctly based on the PHY VPH supply level (1.8V or 1.2V)?			IP Databook, “I2C Pins” section
L5	Review testbench and simulation, (a) Has the phy model been integrated and passed? (b) Are all inputs driven to non "X"? (c) Is your simulation timescale set to 1ns/1ps?			IP Databook, "Integrating the DP AUX PHY in an SoC" section IP Databook, "Integrating the DP AUX-I2C PHY in an SoC" section

	Description	Yes/No	Comments	Reference Materials
L6	Are the voltage levels of power supplies within the reference values?			IP Databook, "Design Implementation Values" section
L7	Ensure there is no inadvertently floating PHY input on ASIC side			N/A
L8	Is the PHY being used in a comboPHY configuration (USB 3.1 and DP Alt mode)? (a) Is the polarity swap signal being controlled correctly?			IP Databook, “DP AUX PHY Settings and Usage” section
L9	Are all other signals set to their default values?			IP Databook, “Signal Descriptions” section

3 Post P&R Static Timing Review

3.1 Post P&R Static Timing Review Checkpoints

Table 3-1 Post P&R Static Timing Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
T1	Is STA performed with the IP timing lib .lib/.db?			IP Databook, "Synopsys .lib and .db Files" section
T2	Is timing closed for best and worst case corners (at least) and setup/hold violations are clean?			STA Flow

4 GDS Review

4.1 GDS Review Checkpoints

Table 4-1 GDS Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
G1	Is the latest released GDS integrated and not modified? Suggest to compare SoC GDS to latest release IP GDS.			Standard Deliverables, GDS file
G2	Are the layers above the IP properly filled? The foundry dummy fill generation utility should be used and DRC should be confirmed to be clean post-fill.			Foundry DRC Rules, Standard Deliverables, Readme file
G3	Is the IP correctly orientated in the SoC?			Foundry DRC Rules
G4	Is the IP placed close to die corner? (a) It is recommended to place the macro at the center of the side of the die.			IP Databook, “Physical-Level Implementation" section IP Databook, “Pad/Package/Board Connections” section
G5	Is there is a keep-out area around the macro boundary? (a) No unrelated routings or devices within 5 µm.			IP Databook, “Physical Implementation Guidelines" section
G6	Are the grounds pins of the PHY connected to the SoC ground supply grid and is the extracted connection resistance below the recommended value?			IP Databook, “Pad/Package/Board Requirements” section IP Databook, "Power Supply Signals" section
G7	Check "cell integrity", (a) No RDL routing from other IPs within the IP area? (b) No routing on top of IP?			N/A

	Description	Yes/No	Comments	Reference Materials
G8	Does routing to IP pins follow these guidelines? (a) Orthogonal to the macro boundary; (b) All the metal layers where the pin is defined are connected (excluding PHY macro side power/ground signals); (c) Connection width is at least same as pin width.			N/A
G9	Is the LVS/DRC sign off deck same as or newer than the SNPS sign off deck?			Standard Deliverables, Readme file
G10	Are the LVS/DRC switch settings as per SNPS recommendations?			Standard Deliverables, Readme file
G11	Does chip-level LVS/DRC pass with the PHY?			Standard Deliverables, Readme file

5 Package Review

5.1 Package Review Checkpoints

Table 5-1 Package Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
P1	Power/Ground Connections (a) Are the VPH and DVDD pins, respectively, isolated on die? (b) Are the grounds common?			IP Databook, "Pad/Package/Board Requirements" section
P2	Are extracted RLC parasitics within recommended values?			IP Databook, "Pad/Package/Board Requirements" section
P3	Are the PADP and PADN signal differential pairs impedance-matched on the package?			IP Databook, "Physical Implementation Guidelines" section
P4	Are the power supplies voltages within the reference value?			IP Databook, "Power and Ground" section

6 PCB Review

6.1 PCB Review Checkpoints

Table 6-1 PCB Review Checkpoints

	Description	Yes/No	Comments	Reference Materials
B1	Are resistors and capacitors with tolerances of 5% and 20%, respectively being used for the PHY AUX_CH_P and AUX_CH_N on board?			VESA DisplayPort Alt Mode on USB Type-C Standard (Section 3.15.1.1)
B2	Are the AUX_CH_P and AUX_CH_N signal differential pairs routed with matching lengths and differential characteristic impedance?			IP Databook, “Physical Implementation Guidelines” section
B3	Are the power supply voltages within the reference value?			IP Databook, "Design Implementation Values" section

7 Testability

7.1 Testability Checkpoints

Note	Access to controllable and observable signals is strongly recommended for complete debugging capabilities.

Table 7-1 Testability Checkpoints

	Description	Yes/No	Comments	Reference Materials
TS1	Are the PHY and control signals controllable and observable for debugging and testing purposes?			IP Databook, “Setting and Using Test Modes” section