SYNOPSYS®

DesignWare® PCIe IP Prototyping Kit

Release Notes

dw_ipk_dwipk_pcie – Product Codes: HW0285-0
HW0297-0
C337-0
HW0370-0
HW0371-0
HW0372-0
HW0373-0

Version 5.10a

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Release Notes: dw_ipk_dwipk_pcie

These release notes describe the changes for 5.10a of the PCIe IP Prototyping Kits listed in "Product Codes".

The following topics are covered:

Product Codes

Table 1-1 lists the products and product codes for the DesignWare PCIe IP Prototyping Kit.

Table 1-1 Product Codes for DesignWare PCIe IP Prototyping Kit

Base Product	Product Code
DesignWare PCIe Gen3 Endpoint Controller on HAPS-DX7, Xilinx Gen3 PHY, with PCIe connection for PC	HW0285-0
DesignWare PCIe Gen3 Root Complex Controller on HAPS-DX7, Xilinx Gen3 PHY, AXI tunnel to ARC SDP	HW0297-0
DesignWare PCIe Gen3 Root Complex Controller on HAPS-DX7, 10G PHY, AXI tunnel to ARC SDP	HW0371-0
DesignWare PCIe Gen3 Endpoint Controller on HAPS-DX7, 10G PHY, PCIe connection for PC	HW0370-0
DesignWare PCIe Gen4 Root Complex Controller on HAPS-DX7, 16G PHY, AXI tunnel to ARC SDP	HW0372-0
DesignWare PCIe Gen4 Endpoint Controller on HAPS-DX7, 16G PHY, PCIe connection for PC	HW0373-0
DesignWare PCIe Gen3 Root Complex IP Soft Prototyping Kit with AXI Tunnel to ARC SDP	C337-0

1.1 New Features and Changes

For the PCIe IP Prototyping Kit feature list see the *DesignWare PCIe IP Prototyping Kit User Guide*.

This reference design tests 5.10a version of the DesignWare Cores PCIe Controller (DWC_pcie_ctl).

The PCIe IP Prototyping Kit was developed and tested with the following PHY Physical Coding Sublayer (PCS) image versions:

- Synopsys C10 PHY board PCS version n100_pciesp1_img0.02
- Synopsys e16 PHY board PCS version 20180202X044_sp1_sg3

Hardware Update

- No update

Software – New Features and Enhancements

- The DesignWare PCIe Root Complex IP Prototyping Kits include the software package (internal) release version dwc_pcie_rc_software_5.10b
- PCIe iATU Unroll Support (DesignWare PCIe Root Complex IP Prototyping Kits)
- The DesignWare PCIe Endpoint Complex IP Prototyping Kits include the software package (internal) release version dwc_pcie_ep_software_5.10b

Software – Bug Fixes

- N/A

1.2 Fixed Defects and Enhancements (STARs on the Web)

You can view a complete list of problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. You must have a SolvNet ID in order to view STAR reports.

You can access STAR reports for any DesignWare verification model or synthesizable component through the IP Directory:

https://www.synopsys.com/designware-ip.html

1.3 Known Issues and Limitations

- The prototype should only be used at room temperature and nominal voltage. The specific hardware you are receiving has only been validated at these conditions.
- Reference design does not support embedded DMA operations.
- The IP Prototyping Kits are to accelerate prototyping, software development, and integration of IP into SoCs. The IP Prototyping Kits were not developed or intended for electrical PHY measurements or compliance testing.
- Equalization Coefficient tests may fail, when using the HAPS-DX7 Xilinx PHY Endpoint IP Prototyping Kit with the Keysight PTC Link Layer tests.

  This is because the transmitter settings of the GTH PHY are not consistent.

  The work-around is to set bit 7 of the DWC_pcie cfg_phy_control register. Setting this bit forces the GTH transmitter settings to be fixed at known good values and allow these tests to pass.
- The BADECRC test may fail, when using the HAPS-DX7 Xilinx PHY and Synopsys e16 PHY board with the Keysight PTC Link Layer tests.
- It is recommended to use a PCIe Analyzer for measuring the throughput. The throughput recorded by PEDA may be inaccurate.
- Timing constraints are not met after running a non-instrumented FPGA Synthesis, when using the DWC_pcie_ctl in Root Complex mode, and the Synopsys e16 SSP PHY.
- tb.pcie_vip_wrapper.VIP_Transceiver error messages are expected. They are caused by the use of an outdated version of Vera VMT.

1.4 Web Resources

- DesignWare IP product information: http://www.designware.com
- Your custom DesignWare IP page: http://www.mydesignware.com
- Documentation through SolvNet: https://solvnet.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): http://www.synopsys.com/keys

1.5 Customer Support

To obtain support for your product contact Support Center using one of the following methods:

- *For fastest response*, use the SolvNet website. If you fill in your information as explained below, your issue is automatically routed to a support engineer who is experienced with your product. The **Product L1** and **Product L2** entries are critical for correct routing.

  Go to http://solvnet.synopsys.com/EnterACall and click on the link to enter a call.
  Provide the requested information, including:

  - **Product L1:** DesignWare IP Prototyping Kits
  - **Product L2:** PCIe
  - **Product L3:** dw_ipk_dwipk_pcie
  - **Problem Type:**
  - **Priority:**
  - **Title:** Provide a brief summary of the issue or list the error message you have encountered
  - **Description:** For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):

  - Include the Product name, Sub Product name, and Tool Version number in your e-mail (as identified above) so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood

- Or, telephone your local support center:

  - North America:

    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.

  - All other countries:

    https://www.synopsys.com/support/global-support-centers.html

1.6 Previous Releases

1.6.1 Release 3.00a

Hardware Update

- PCIe 4.0 PHY Board

Software – New Features and Enhancements

- The DesignWare PCIe Root Complex Gen3 IP Prototyping Kit includes the software package (internal) release version dwc_pcie_rc_software_4.80a
- PCIe iATU Unroll Support (DesignWare PCIe Root Complex Gen3 IP Prototyping Kit)
- The DesignWare PCIe Endpoint Complex Gen3 IP Prototyping Kit includes the software package (internal) release version dwc_pcie_ep_software_4.80a
- DMA Unroll Support (DesignWare PCIe Endpoint Complex Gen3 IP Prototyping Kit)

Software – Bug Fixes

- Not available