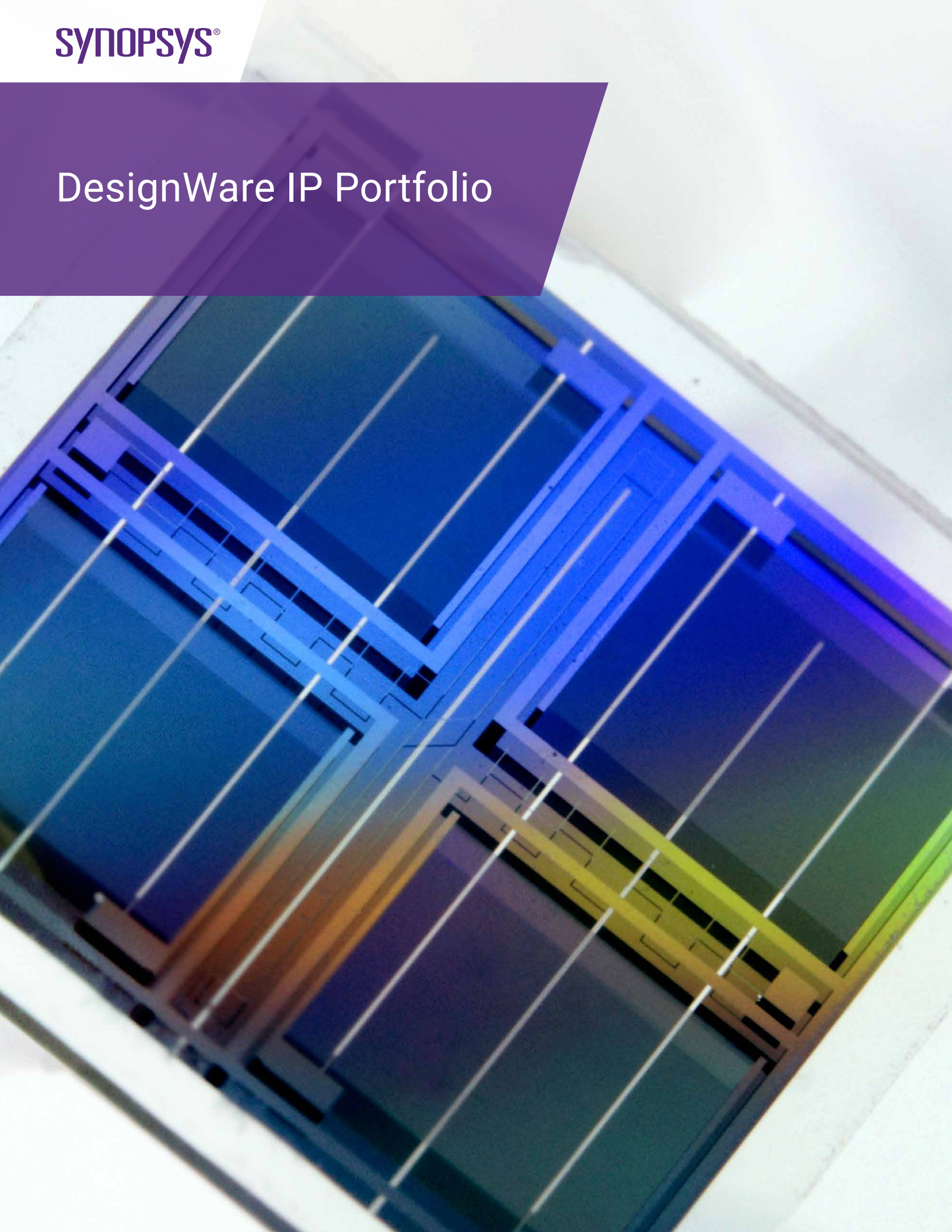
SYNOPSYS®

DesignWare IP Portfolio



Broad IP Portfolio

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare® IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, interface IP, security IP, embedded processors and subsystems.

To accelerate your product development cycle, Synopsys' IP Accelerated initiative offers SoC architecture design support, IP subsystems, signal integrity/power integrity analysis and IP hardening, IP prototyping kits, and comprehensive silicon bring-up support.

Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

Interface IP												
USB	Process Technologies										Controllers/ Features	Verification IP
	65 nm	55 nm	40/45 nm	28 nm	22 nm	20 nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET		
USB 3.1							✓	✓			Dual-Role Device (Device & Host)	✓
USB-C 3.1				In Dev.			✓	✓		✓	Dual-Role Device (Device & Host)	✓
USB-C 3.1/ DisplayPort 1.4					In Dev.			✓		✓	Device, Host, Transmit, DisplayPort Tx	✓
USB-C 3.1/ DisplayPort 1.3					In Dev.		✓	✓	✓	✓	Dual-Role Device (Device & Host), Transmit, DisplayPort Tx	✓
USB 3.0	✓	✓	✓	✓	In Dev.	✓	✓	✓			Dual-Role Device, Device, Host, SSIC, HSIC	✓
USB-C 3.0				✓			✓	✓			Device, Host	✓
USB 2.0	✓	✓	✓	✓	In Dev.	✓	✓	✓	✓	✓	Device, Host, HSIC, Dual-Role Device	✓
USB-C 2.0	✓	✓	✓	✓	In Dev.	✓	✓	✓	✓	✓	Device, Host, Dual-Role Device	✓
HSIC			✓	✓		✓	✓		✓		Device, Host	✓

PCI Express	Process Technologies										Controllers	Configu-ration	Verifica-tion IP
	65 nm	55 nm	40/45 nm	28 nm	22 nm	20 nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET			
PCIe 5.0							In Dev.			In Dev.	Endpoint, Root Port, Dual Mode, Switch	x1, x2, x4, x8, x16	✓
PCIe 4.0				✓			✓	✓		✓	Endpoint, Root Port, Dual Mode, Switch	x1, x2, x4, x8, x16	✓
PCIe 3.1				✓	In Dev.		✓	✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch	x1, x2, x4, x8, x16	✓
PCIe 2.1	✓	✓	✓	✓	In Dev.	✓	✓	✓		✓	Endpoint, Root Port, Dual Mode, Switch	x1, x2, x4, x8, x16	✓
PCIe 1.1	✓	✓	✓	✓		✓	✓				Endpoint, Root Port, Dual Mode, Switch	x1, x2, x4, x8, x16	✓

Interface IP

CCIX	Process Technologies									Controllers	Verification IP
	65 nm	55 nm	40/45 nm	28 nm	20 nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET		
CCIX						✓			✓	Endpoint, Root Port, Dual Mode, Switch	✓

HDMI	Process Technologies										Controllers	Verification IP
	65 nm	55 nm	40/45 nm	28 nm	22 nm	20 nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET		
HDMI 2.1							✓	✓			✓	✓
HDMI 2.0			✓	✓	In Dev.		✓	✓			✓	✓
HDMI 1.4	✓	✓	✓	✓							✓	✓

DDR	Process Technologies									Controllers	Platform Architect Support	Verifica-tion IP
	65 nm	55 nm	40/45 nm	28 nm	20 nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET			
LPDDR5						In Dev.	In Dev.		In Dev.	In Dev.	In Dev.	✓
LPDDR4				✓		✓	✓	✓	✓	Protocol controller, Memory controller	✓	✓
LPDDR4X				✓		✓	✓		✓	Protocol controller, Memory controller	✓	✓
LPDDR3			✓	✓		✓	✓	✓		Protocol controller, Memory controller	✓	✓
LPDDR2	✓		✓	✓		✓				Protocol controller, Memory controller	✓	✓
DDR5						In Dev.	In Dev.		In Dev.	In Dev.		✓
DDR4			✓	✓		✓	✓	✓	✓	Protocol controller, Memory controller	✓	✓
DDR3	✓	✓	✓	✓		✓	✓	✓		Protocol controller, Memory controller	✓	✓
DDR2	✓	✓	✓	✓						Protocol controller, Memory controller	✓	✓

HBM	Process Technologies									Controllers	Verification IP
	65 nm	55 nm	40/45 nm	28 nm	20 nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET		
HBM2						In Dev.	In Dev.		✓	In Dev.	✓

Interface IP										
MIPI	Process Technologies								Controllers	Verification IP
	40/45 nm	28 nm	22 nm	20 nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET		
D-PHY	✓	✓	In Dev.	✓	✓	✓		✓	CSI-2, DSI	✓
M-PHY		✓	In Dev.		✓	✓	✓	✓	UFS, UniPro	✓
CSI-2									Host, Device	✓
DSI									Host, Device	✓
DSI + DSC									DSI + DSC Encoder	✓
UniPro									v1.6, v1.8	✓
I3C									Master, Slave, Slave Lite	✓

Ethernet	Process Technologies			PCS	Controllers	Verification IP
	28nm	14/16nm FinFET	7nm FinFET			
RXAUI/Double XAUI (6.25 G)	✓	✓	✓	✓	✓	✓
1000BASE-KX, Energy Efficient Ethernet, 10GBASE-KR, 10GBASE-KX4	✓	✓	✓	✓	✓	✓
40GBASE-KR4, 40GBASE-CR4, XLAUI	✓	✓	✓	✓	✓	✓
100GBASE-CR10, CAUI	✓	✓	✓	✓	✓	✓
SGMII	✓	✓	✓	✓	✓	✓
QSGMII	✓	✓	✓	✓	✓	✓
XFI, SFI (SFF-8431)	✓	✓	✓	✓	✓	✓
GMII/MII, RGMII, RTBI, TBI, SMII, RMII, RevMII, XGMII, XLGMII				✓	✓	✓
IEEE TSN/AVB Standards: IEEE 802.1AS, 802.1AS-Rev, 802.1Qav, 802.1Qat, 802.1Qbv, 802.1Qbu & 802.3br					✓	✓
25G/50G Ethernet Consortium and IEEE specifications		✓	✓	✓	✓	✓
2.5G/5.0G USXGMII		✓	✓	✓	✓	✓
Additional Enterprise Protocols						
OIF, CEI-6G/11G	✓	✓	✓			
CPRI, OBSI, JESD204 A/B	✓	✓	✓			✓
SRIO	✓	✓	✓			

SATA	Process Technologies						Controllers	Verification IP
	65nm	55nm	40/45nm	28nm	14/16nm FinFET	7nm FinFET		
SATA 6G	✓	✓	✓	✓	✓	In Dev.	Host, Device	✓
SATA 3G	✓	✓	✓	✓	✓	In Dev.	Host, Device	✓

Bluetooth Low Energy	Process Technologies				Link Layer (Controller)/ MAC (HW, FW)
	180nm	55nm	40nm	22nm	
Bluetooth 5	✓	✓	✓	In Dev.	✓
IEEE 802.15.4		✓	✓	In Dev.	In Dev.

Interface IP

Mobile Storage	Process Technologies						Controllers	Verification IP
	28nm	22nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET		
UFS							✓	✓
UniPro							✓	✓
M-PHY	✓		✓	✓	✓	✓	✓	✓
eMMC	✓	In Dev.	✓	✓			✓	✓
SD	✓	In Dev.	✓	✓			✓	✓
SDIO	✓	In Dev.	✓	✓			✓	✓

AMBA	Synthesizable IP	Verification IP
AXI 3 and AXI 4 bus fabric, bridges, and infrastructure IP	✓	✓
AHB and AXI DMA controllers	✓	✓
AMBA peripherals (SSI for SPI/ xSPI bus, I^2C, I^2S, UART)	✓	✓
Timers, interrupt controllers, GPIOs, interconnect matrices	✓	✓

Datapath IP	Synthesizable IP	Simulation Models (C++, Verilog)	Verification Models
Floating point functions	✓	✓	✓
Fixed point functions	✓	✓	✓
Trigonometric functions	✓	✓	✓

Analog IP

Data Converters	Process Technologies									Bits	MSPS	Channel Configu-ration
	180nm	130nm	90nm	65nm	55nm	40nm	28nm	22nm	12/16nm FinFET			
>100 MHz ADCs	✓			✓		✓	✓	In Dev.	✓	10, 12	110 to 320	Single, Dual
40-100 MHz ADCs				✓		✓	✓	In Dev.	✓	10, 12	40 to 100	Single, Dual
4-40 MHz ADCs			✓	✓	✓	✓	✓	In Dev.	✓	10, 12	5 to 25	Single, Dual
<4 MHz ADCs	✓	✓	✓	✓	✓	✓				10, 12, 14, 16	1 to 2	Single
Communications DACs				✓		✓	✓	In Dev.	✓	10, 12	80 to 640	Single, Dual
Auxiliary DACs				✓		✓	✓	In Dev.	In Dev.	11, 12	20	Single
Video DACs		✓		✓		✓	✓			10	170 to 300	1 to 6

Audio Analog Codecs	Process Technologies									Bits	Dynamic Range	Sam-pling Rate
	180nm	130nm	90nm	65nm	55nm	40nm	28nm	22nm	12/16nm FinFET			
Advanced Audio Analog Codecs						✓				24	96dB	8 to 192kHz
Premium Audio Analog Codecs							✓			24	96dB	8 to 192kHz

Memories and Logic Libraries								
Embedded Memories	Process Technologies							
	65nm	55nm	40/45nm	28nm	22nm	14/16nm FinFET	12nm FinFET	7nm FinFET
High-Density Single Port SRAM, High-Density Dual Port SRAM	✓	✓	✓	✓	In Dev.	✓	✓	In Dev.
High-Density 1P RF, High-Density 2P RF	✓	✓	✓	✓	In Dev.	✓	✓	✓
High-Density ROM	✓	✓	✓	✓	In Dev.	✓	✓	✓
High-Speed Single Port SRAM	✓	✓	✓	✓	In Dev.	✓	✓	✓
High-Speed Dual Port SRAM	✓	✓	✓	✓	In Dev.	✓	✓	
High-Speed 1P RF (Cache)	✓	✓	✓	✓	In Dev.	✓	✓	✓
High-Speed Asynchronous 2-Port Register File			✓	✓	In Dev.	✓		
UHD 1P RF								✓
UHD 2P RF	✓	✓	✓	✓	In Dev.	✓	✓	✓
UHD 2P SRAM				✓	In Dev.	✓		✓
STAR Memory System Embedded Test and Repair	✓	✓	✓	✓	✓	✓	✓	✓
STAR Hierarchical Test	✓	✓	✓	✓	✓	✓	✓	✓

Logic Libraries	Process Technologies							
	65nm	55nm	40/45nm	28nm	22nm	14/16nm FinFET	12nm FinFET	7nm FinFET
High-Speed Library	✓	✓	✓	✓	In Dev.	✓	✓	✓
High-Speed Multi-channel			✓	✓	In Dev.	✓	✓	✓
High-Speed POK	✓	✓	✓	✓	In Dev.	✓		✓
High-Density Library	✓	✓	✓	✓	In Dev.	✓		✓
High-Density Multi-channel			✓	✓	In Dev.	✓		✓
High-Density POK	✓	✓	✓	✓	In Dev.	✓		✓
UHD Library, UHD POK	✓	✓	✓	✓	In Dev.	✓	✓	✓
UHD Multi-channel			✓	✓	In Dev.	✓	✓	✓
Ultra-low leakage (thick oxide)			✓		In Dev.	In Dev.	In Dev.	
High-Performance Core Design Kit			✓	✓	In Dev.	✓	✓	✓
Enhanced Reliability Kit						✓		

Non-Volatile Memory	Process Technologies								Bit Counts	Endurance (Write Cycles)
	152/ 180nm	110/ 130nm	80/90 nm	55/65 nm	40 nm	28nm	14/16nm FinFET	7nm FinFET		
One-Time Programmable (OTP)	✓	✓	✓	✓	✓	✓	✓	✓	16 bit to 1 Mbit	1 per instance
Multi-Time Programmable (MTP) Medium-Density	✓	In Dev.							16 bit to 256 Kbit	Up to 10,000
MTP EEPROM	✓	✓	✓ (90nm)	✓	✓				128 bit to 8 Kbit	Up to 1,000,000
MTP ULP	✓	In Dev.							128 bit to 4 Kbit	Up to 100,000
Few-Time Programmable Trim	✓	✓							64 bit to 2 Kbit	Up to 10,000

Security IP		
Security	Synthesizable IP	Software
Cryptography IP	✓	✓
Security Protocol Accelerators	✓	✓
Hardware Secure Modules with Root of Trust	✓	✓
Content Protection IP	✓	✓

Accelerate Development of Performance-Efficient SoCs

Synopsys' DesignWare ARC® Processors are a family of 32-bit CPUs that SoC designers can optimize for a wide range of uses, from deeply embedded to high-performance host applications in a variety of market segments. Designers can differentiate their products by using patented configuration technology to tailor each ARC processor instance to meet specific performance, power and area requirements. The DesignWare ARC processors are also extendable, allowing designers to add their own custom instructions that dramatically increase performance. Synopsys' ARC processors have been used by over 230 customers worldwide who collectively ship more than 1.9 billion ARC-based chips annually.

All DesignWare ARC processors utilize a 16-/32-bit ISA that provides excellent performance and code density for embedded and host SoC applications. The RISC microprocessors are synthesizable and can be implemented in any foundry or process, and are supported by a complete suite of development tools.

DesignWare ARC processors are supported by a broad ecosystem of commercial and open source tools, operating systems and middleware. This includes offerings from leading industry vendors who are members of the ARC Access Program as well as a comprehensive suite of free and open source software available through the embARC Open Software Platform.

Processor IP								
ARC 32-bit Processors	Max CCM Size	Cache Size	DSP	MPU	Enhanced Security Package	MMU	Floating Point	Trace
EM4	2MB			✓	✓		✓	✓
EM6	2MB	32K		✓	✓		✓	✓
EM5D	2MB		✓	✓	✓		✓	✓
EM7D	2MB	32K	✓	✓	✓		✓	✓
EM9D	2MB		✓	✓	✓		✓	✓
EM11D	2MB	32K	✓	✓	✓		✓	✓
EM4SI	2MB			✓			✓	✓
EM5DSI	2MB		✓	✓			✓	✓
SEM110	2MB			✓			✓	
SEM120D	2MB		✓	✓			✓	
605 LE	512KB			✓				
710D	512KB		✓	✓			✓	✓
725D	512KB	64K	✓	✓			✓	✓
770D	512KB	64K	✓	✓		✓	✓	✓
610D	512KB		✓	✓			✓	✓
625D	512KB	32K	✓	✓			✓	✓
AS211SFX	512KB	32K	✓	✓			✓	✓
AS221BD (dual-core)	512KB ea core	32K ea core	✓	✓			✓	✓

Processor IP								
ARC HS 32-bit Processors	Max CCM Size	Cache Size	DSP	L1 Coherency	L2 Cache	MMU	Floating Point	Trace
HS34, HS34x2, HS34x4	16MB						✓	✓
HS36, HS36x2, HS36x4	16MB	64K		✓			✓	✓
HS38, HS38x2, HS38x4	16MB	64K		✓	8MB	✓	✓	✓
HS44, HS44x2, HS44x4	16MB						✓	✓
HS46, HS46x2, HS46x4	16MB	64K		✓			✓	✓
HS48, HS48x2, HS48x4	16MB	64K		✓	8MB	✓	✓	✓
HS45D, HS45Dx2, HS45Dx4	16MB		✓				✓	✓
HS47D, HS47Dx2, HS47Dx4	16MB	64K	✓	✓			✓	✓

Embedded Vision Processors	CNN Engine (MACs)	Vision CPU MACs	DMA	32-bit Scalar	512-bit Vector DSP	L1 Cache Coherency	FPU
EV61	880, 1,760 or 3,520	64	✓	1	1		✓
EV62	880, 1,760 or 3,520	128	✓	2	2	✓	✓
EV64	880, 1,760 or 3,520	256	✓	4	4	✓	✓

IP Accelerated Initiative

With IP Accelerated, Synopsys has augmented its broad portfolio of silicon-proven DesignWare IP with SoC architecture design support, IP subsystems, signal integrity/power integrity analysis and IP hardening, IP prototyping kits, and comprehensive silicon bring-up support to accelerate your product development cycle.

IP Subsystems				
ARC Processor IP Subsystems	Supported ARC Processors	Hardware Accelerators	Integrated Peripherals	Included Software
Secure IP Subsystem	SEM110, SEM120D	✓	UART, TRNG I/F, Device ID, NVM I/F, GPIO	Crypto library, DSP library (SEM120D), device drivers, secure boot, SecureShield runtime library
Data Fusion IP Subsystem	EM5D, EM7D, EM9D, EM11D	✓	SPI, I²C, I²S, I3C, UART, PDM, ADC I/F, APB I/F, GPIO	DSP library, audio processing library, peripheral I/O drivers (bare metal), reference designs
Sensor and Control IP Subsystem	EM4, EM6	✓	SPI, I²C, PWM, UART, ADC I/F, DAC I/F, APB I/F, GPIO	DSP library, motor control library, peripheral I/O drivers (bare metal), reference designs
SoundWave Audio Subsystem	AS211SFX, AS221BD	✓	I²S, S/PDIF, analog codec I/F, reset, clock management	Multi-core media framework, MM MQX audio post-processing software

Interface IP Subsystems	Supported IP	Multiprotocol Support	Integrated Logic	Included Scripts
IP Protocol-Specific Subsystems	USB, PCIe, DDR, Ethernet, HDMI, MIPI, AMBA, Security	✓	AMBA or native bus, clock management, reset, DMA, interrupts, memory, power management, debug and test logic, switches	Configuration scripts, test environment, test scripts, implementation scripts

IP Prototyping Kits and Software Development Kits							
Protocol/Standard	IP Prototyping Kit with ARC SDP			IP Prototyping Kit with PCIe Connection to PC			IP Prototyping Kit for Arm Juno Development Board
	HW Based	Soft Deliverable		HW Based	Soft Deliverable		Hardware Based
	HAPS-DX	HAPS-DX	HAPS-80	HAPS-DX	HAPS-DX	HAPS-80	HAPS-DX
USB 3.1 Host				✓	✓	✓	
USB 3.1 Device				✓		✓	
USB 3.0 Host	✓			✓		✓	✓
USB 3.0 Device	✓			✓		✓	
USB 3.0 Dual-Role Device				✓			
USB 2.0 Dual-Role Device				✓			
DisplayPort 1.3 TX				✓	✓		
PCIe 4.0 Endpoint				✓			
PCIe 4.0 Root Complex	✓						
PCIe 3.1 Endpoint				✓		✓	
PCIe 3.1 Root Complex	✓	✓	✓				
PCIe 2.1 Endpoint				✓		✓	
PCIe 2.1 Root Complex			✓				
DDR 4/3	✓	✓	✓				
LPDDR 4/3	✓	✓	✓				
HDMI 2.0 TX	✓			✓			
HDMI 2.0 RX	✓						
Ethernet QoS				✓	✓		
Ethernet XGMAC				✓			
JEDEC UFS Host	✓		✓	✓			
SD/eMMC				✓			
MIPI CSI-2 Host	✓						
MIPI CSI-2 Device	✓		✓				
MIPI DSI Host	✓		✓				
MIPI DSI Device				✓			
I3C Multi-Role (Master/Slave)	✓						
SATA 6G Host				✓			
SATA 6G Device	✓			✓			

For more information on DesignWare IP, visit synopsys.com/designware.

SYNOPSYS®
Silicon to Software™

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