**Broad IP Portfolio**

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, In-chip PVT monitors, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems.

To accelerate your product development cycle, Synopsys' IP Accelerated initiative offers SoC architecture design support, IP subsystems, signal integrity/power integrity analysis and IP hardening, IP prototyping kits, and comprehensive silicon bring-up support.

Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

<table>
<thead>
<tr>
<th>USB</th>
<th>Processes</th>
<th>Controllers/Features</th>
<th>HS Access &amp; Test</th>
<th>Verification IP</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB4</td>
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<td>Device, Router, Host Router</td>
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<td>Device, Host, DisplayPort Tx, HDCP ESM, DSC</td>
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<tr>
<th>MIPI</th>
<th>Process Technologies</th>
<th>Controllers</th>
<th>Verification IP</th>
<th>Auto Grade</th>
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## Interface IP

### PCI Express

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<tr>
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<th>Controllers</th>
<th>Configuration</th>
<th>IDE Security Module</th>
<th>HS Access &amp; Test</th>
<th>Verification IP</th>
<th>Auto Grade</th>
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### HDMI

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<td>DP 1.4</td>
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### CXL

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### CCIX

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### HBM

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### Ethernet

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<td>28nm</td>
<td>14/16nm FinFET</td>
<td>7nm FinFET</td>
<td>5nm FinFET</td>
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<td>✔️</td>
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<td>Process Technologies</td>
<td>Controllers</td>
<td>Verification IP</td>
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<td>Controller (Link Layer / MAC)</td>
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<td><strong>AMBA</strong></td>
<td>Synthesizable IP</td>
<td>Verification IP</td>
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<tr>
<td>AMBA APB 3/4, AHB 2/5, AXI 3/4</td>
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<td>AHB and AXI DMA Controllers</td>
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<td>SSI Controller (SPI/xSPI)</td>
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## Analog IP

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<th>Process Technologies</th>
<th>Bits</th>
<th>MSPS</th>
<th>Channel Configuration</th>
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## Foundation IP

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<th>Process Technologies</th>
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<th>55nm</th>
<th>40/45nm</th>
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<th>10nm FinFET</th>
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*Available in Consumer and Automotive
## Foundation IP

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<tr>
<th>Logic Libraries</th>
<th>Process Technologies</th>
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<td>High-Speed POK</td>
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<td>UHD POK</td>
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<tr>
<td>Ultra-low leakage (thick oxide)</td>
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</table>

*Available in Consumer and Automotive

## I/O Products

<table>
<thead>
<tr>
<th>I/O Products</th>
<th>22nm</th>
<th>14/16nm FinFET</th>
<th>12nm FinFET</th>
<th>6/7nm FinFET</th>
<th>5nm FinFET</th>
<th>4nm FinFET</th>
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## Non-Volatile Memory

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<th>150/180nm</th>
<th>110/130nm</th>
<th>80/90nm</th>
<th>55/65nm</th>
<th>40nm</th>
<th>28nm</th>
<th>22nm</th>
<th>14/16nm FinFET</th>
<th>12nm FinFET</th>
<th>Bit Counts</th>
<th>Endurance (Write Cycles)</th>
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<td>✓</td>
<td>✓</td>
<td>16 bit to 1 Mbit</td>
<td>1 per instance</td>
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<td>64 bit to 4 Kbit</td>
<td>Up to 1,000</td>
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## In-Chip PVT Monitoring IP

<table>
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<th>28nm</th>
<th>16nm FinFET</th>
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<th>7nm FinFET</th>
<th>6nm FinFET</th>
<th>5nm FinFET</th>
<th>3nm FinFET</th>
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<td>Temperature Sensor</td>
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<tr>
<td>Distributed Thermal Sensor</td>
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| Soft IP                   |      |             |             |            |            |            |            |
| PVT Controller            | ✓    | ✓           | ✓           | ✓          | ✓          | ✓          | ✓          |
| Software Driver           | ✓    | ✓           |             | ✓          | ✓          | ✓          | ✓          |
Path Margin Monitor IP

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<th>Synthesizable IP</th>
<th>Software</th>
<th>Safety Compliant</th>
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<td>Security Protocol Accelerators</td>
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<td>Hardware Secure Modules with Root of Trust</td>
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<td>DDR/LPDDR Inline Memory Encryption IP</td>
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Accelerate Development of Performance-Efficient SoCs

Synopsys ARC® Processors are a family of 32-/64-bit CPUs and DSPs that SoC designers can optimize for a wide range of uses, from deeply embedded to high-performance host applications in a variety of market segments. Designers can differentiate their products by using patented configuration technology to tailor each ARC processor instance to meet specific performance, power and area requirements. The Synopsys ARC processors are also extensible, allowing designers to add their own custom instructions that dramatically increase performance. Synopsys’ ARC processors have been used by over 275 customers worldwide who collectively ship more than 2.5 billion ARC-based chips annually.

All Synopsys ARC processors utilize a 16-/32-/64-bit ISA that provides excellent performance and code density for embedded and host SoC applications. The RISC and DSP processors are synthesizable and can be implemented in any foundry or process, and are supported by a complete suite of development tools.

Synopsys ARC processors are supported by a broad ecosystem of commercial and open source tools, operating systems and middleware. This includes offerings from leading industry vendors who are members of the ARC Access Program as well as a comprehensive suite of free and open source software available through embARC.org.

Processor IP

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<th>Max CCM Size (I&amp;D)</th>
<th>Cache Size (I&amp;D)</th>
<th>DSP</th>
<th>MPU</th>
<th>Safety Certified</th>
<th>Enhanced Security Package</th>
<th>MMU</th>
<th>Floating Point</th>
<th>Trace</th>
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synopsys.com/ip
### Processor IP

**ARC HS**

<table>
<thead>
<tr>
<th>32-bit Processors</th>
<th>Max CCM Size</th>
<th>L1 Cache (I &amp; D)</th>
<th>DSP</th>
<th>Safety Certified</th>
<th>L1 Coherency</th>
<th>L2 Cache</th>
<th>MMU</th>
<th>Floating Point</th>
<th>Trace</th>
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<tbody>
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### ARC HS

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<th>Max CCM Size</th>
<th>L1 Cache (I &amp; D)</th>
<th>L1 Coherency</th>
<th>Shared L2 Cache/Cluster Mem.</th>
<th>MMU</th>
<th>Floating Point</th>
<th>Trace</th>
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### ARC VPX DSP

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<th>Vector Execution Unit</th>
<th>Vector Length</th>
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<th>Dual Floating Point Vector Engine (optional)</th>
<th>Floating Point Vector Math Engine (optional)</th>
<th>Safety Certified</th>
<th>L1 Coherency</th>
<th>Multicore configurations</th>
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### ARC NPX

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<th>MACs</th>
<th>DMA</th>
<th>L2 Shared Memory</th>
<th>L2 Controller</th>
<th>Tensor Accelerator</th>
<th>Tensor Floating Point Unit (FPU) (optional)</th>
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<th>Memory Management Unit (MMU)</th>
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IP Accelerated Initiative

With IP Accelerated, Synopsys has augmented its broad portfolio of silicon-proven Synopsys IP portfolio with SoC architecture design support, IP subsystems, signal integrity/power integrity analysis and IP hardening, IP prototyping kits, and comprehensive silicon bring-up support to accelerate your product development cycle.

IP Subsystems support many protocols and deliverables for IP integration including configuration scripts, test environment, test scripts, linting, CDC checks, RDC checks, synthesis scripts and implementation scripts. The subsystems also include AMBA or native bus, clock management, reset, DMA, interrupts, memory, power management, debug and test logic.

Hardening and SIPI provide a GDSII for integration in an SoC and include On-chip decoupling capacitance, power and ground pins, PHY & SDRAM termination strategy, SoC package design, PCB stack-up and trace width/spacing, performance at required data rate, read/write/address, and command/control timing budgets.

With your vision and our expertise, we can tune IP to your SoC, enabling your team to focus on product differentiation.
## IP Subsystems

<table>
<thead>
<tr>
<th>Interface IP Subsystems</th>
<th>Auto Grade</th>
<th>UVM</th>
<th>Spyglass</th>
<th>SRAM/MBIST</th>
<th>UPF</th>
<th>DFT</th>
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## Configurable IP Subsystems

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## Signal/Power Integrity Analysis & IP Hardening

### Supported IP

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<thead>
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<th>Multi-Protocol Support</th>
<th>Consultation Expertise</th>
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<td>DDR, LPDDR, HBM, PCIe, USB, MIPI, Ethernet, HDMI</td>
<td>On-chip decoupling capacitance, power and ground pins, PHY &amp; SDRAM termination strategy, SoC package design, PCB stack-up and trace width/spacing, performance at required data rate, read/write/address, command/control timing budgets</td>
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### IP Hardening

<table>
<thead>
<tr>
<th>Supported IP</th>
<th>Multi-protocol Support</th>
<th>Synthesis to GDSII</th>
<th>Floor Planning</th>
<th>Scan Insertion</th>
<th>Power Grid</th>
<th>Skew Balancing</th>
<th>RDL Routing</th>
<th>Bump Assignment</th>
<th>IR/EM-Analysis</th>
<th>DRC/LVS</th>
<th>GLS</th>
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## Signal/Power Integrity Analysis

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<thead>
<tr>
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<th>Multi-protocol Support</th>
<th>Floorplan Review</th>
<th>Pre/Post Layout Analysis</th>
<th>Decap Cell Size/Placement</th>
<th>Power Impedance Simulations</th>
<th>Eye Quality Analysis</th>
<th>End to End Analysis</th>
<th>Timing Budget Analysis</th>
<th>Signal Quality PVT Corner Analysis</th>
<th>Full Report</th>
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For more information on Synopsys IP, visit synopsys.com/ip.