SYNOPSYS®
Accelerating Innovation

DesignWare IP for Mobile SoC Designs

Mobile Devices Leading the Consumer Market

The sales of mobile devices continue to lead the consumer electronics market, with about 97% of adults aged 18-34 in the United States owning a mobile phone[1]. The majority of these adults will replace these phones frequently as manufacturers release new devices with more features, faster performance and longer battery life. Gartner predicts that over 2 billion mobile phones will ship in 2016[2]. Furthermore, mobile phone ownership is expanding to developing countries with 1.28 billion mobile users in China[3].

The mobile market can be categorized into four key segments including super phones/ phablets, high-end notebooks/tablets, low-cost phones and lost-cost tablets. All of these devices incorporate distinguished features and have different design requirements, making mobile designs more dynamic and complex.

How Mobile Device Manufacturers are Responding

Mobile device manufacturers are responding to this growth by giving consumers more of everything - larger, higher resolution screens, faster wireless modems, faster WiFi, better connectivity to nearby devices and wearables, faster processors, more memory, more storage, better cameras, better software, better sound, more connectivity to external displays, and better security. These features must be provided, while considering the demands for longer battery life and thinner form factors.

The Impact on Mobile SoC Design

With the continuous push to develop differentiated products, designers are faced with the challenges of how to incorporate the latest technologies into their chips more quickly, cost-effectively and with less risk. As the functionality grows, so does the complexity of these SoCs. Designers need to address critical requirements such as achieving the highest performance with lowest power consumption, integrating new connectivity standards and moving to smaller process technologies.

Lowering Power

Controlling power consumption is critical in mobile devices. With today's constant on-the-go lifestyle and the need to be connected at all times, having a device that cannot last a reasonable time between charges is unacceptable. At the same time, a device with an unreasonably large battery may be too heavy, too thick, or too expensive for most consumers.

A mobile device may support a number of power states, and each component within the device may also have different power states. Examples of power states include:

- "Fully On", where the device or component is operating at its maximum potential. Many devices or components will only use this state for a small fraction of the time, for example, when playing an action game or moving a large amount of data between components
- A number of "Partially On" states, where the device or component is operating at a reduced potential corresponding to a lower demand on the mobile device such as web-browsing or listening to music.
- "Idle", where the device or component is on but not being actively used.
- "Standby", where the device is dark and in the user's pocket, even though it may be in the "Always On, Always Connected" mode. This means that some part of the device is constantly monitoring for new input and maintaining periodic contact with wireless, WiFi, or personal-area networks

The challenge for any mobile device manufacturer is to enable a rich user experience, particularly in the "Fully On" state, which tends to drive the device replacement cycle, while controlling power in every component to extend battery life.

Synopsys provides a range of design IP that helps address the low power requirements of mobile devices including the following:

- Low latency, multi-port memory controllers and PHYs optimized to control power while supporting the latest low-power DDR memory standards
- MIPI D-PHY and M-PHY physical layers operating at speeds up to 5.8 Gb/s and multiple power states
- MIPI controllers that connect to Displays (DSI), Cameras (CSI), Storage (UFS), RF ICs (DigRF), UniPro, and other common mobile device components
- USB 2.0, 3.0 and 3.1 controllers and PHYs that provide high-speed connections to external USB peripherals
- Controllers and PHYs for chip-to-chip connections inside the mobile device, such as M-PCIe/M-PHY, USB-SSIC/M-PHY, and USB-High-Speed Inter-Chip (HSIC)
- Controllers and PHYs for HDMI connections to external displays up to 4K Ultra High Definition resolution
- Embedded memories and logic libraries optimized for maximum performance with the lowest possible power consumption
- Analog Front End (AFE) for analog data reception and interchip communication of analog data
- Controllers and PHYs for PCI Express®, SATA, and Ethernet interfaces used in notebook devices
- An integrated hardware and software audio subsystem
- Fundamental building blocks and ARM®AMBA® on-chip-bus peripherals

Accelerating Mobile SoC Designs with IP

Driven by short product development cycles, demand for new features and rapidly changing standards, SoC designers are relying on high-quality, 3rd party IP from trusted providers to reduce integration risk and accelerate time-to-market.

Mobile device IC architects and designers need optimized IP solutions that are specifically designed to meet system requirements for mobile applications. Typical system requirements include high-speed and low-power connections between the application processor, baseband IC or modem, wireless interface chips, and mobile peripheral devices.

Synopsys' low latency, mission critical IP solutions enable efficient communications throughout the SoC using standard on-chip bus interconnects such as ARM® AMBA® 4 AXI® and AMBA 3 AXI.

Synopsys provides a comprehensive portfolio of high quality IP solutions that enable designers to develop SoCs for applications such as mobile phones, tablets, notebooks, and wearable devices. The silicon-proven DesignWare IP and prototyping solutions are optimized for high-performance, low power and low latency, and supports advanced process technologies from 28-nm to 16-nm/14-nm FinFET.

DesignWare IP for Mobile Devices

DesignWare IP	Product Features for Mobile SoCs	Mobile SoC Impact
Low-Power DDR (LPDDR) Controller and PHY	Low latency, high-bandwidth, multi-port memory controller and PHY supporting the highest speeds, up to 3200 Mbps of the latest generation low power LPDDR devices	Application processors can use multiple ports and Quality-of-Service (QoS) functions to optimize memory traffic across the SoC, while controlling power with automated power states
MIPI D-PHY and M-PHY	2-lane D-PHY up to 1.5 Gbps and GEAR3 M-PHY up to 5.8 Gbps support high-speed chip-to-chip and chip-to-device interconnect with very low mW/GHz	Multi-lane, multi-geared interfaces enable optimal matching of data rate and power usage
MIPI DSI, CSI-2, UFS, DigRF and UniPro Controllers	MIPI controllers that connect to Displays, Cameras, Storage, RF ICs, and other common mobile device components	Enables integration of a range of MIPI interfaces into baseband and application processor ICs
USB and M-PCIe Controllers	USB HSIC, USB 3.0 SSIC and M-PCIe with MIPI M-PHY for inter-chip communication	Allows high-speed asymmetric inter-chip communication with application-optimized bandwidth and power
USB 3.1, USB 3.0 and USB 2.0 Controllers and PHYs	Low-power features with USB 3.1 operating at 10 Gbps, SuperSpeed USB 3.0 operating at 5 Gbps and high-speed USB 2.0	Enables fast synching and data transfer from mobile devices to host computers and storage
SATA 6G Host and Device Controllers and PHY	AHCI programming model support multiple ports. Integrated DMA and advanced power management	Provides lower latency and higher bandwidth data transfers for notebooks and enables low-power operation
HDMI 2.0 TX and RX Controllers and PHYs	6 Gbps per lane supports 4K Ultra High Definition at up to 60 FPS with low power	Enables display of mobile device content on external monitors and TVs
Embedded Memories and Logic Libraries	High Performance Core Design Kit optimized for all processor cores on SoC: CPU, GPU and DSP cores; STAR Memory system with ECC support	Enables optimal implementation across all three dimensions: performance, power, and area.
Analog Front End IP	Analog-to-digital and digital-to-analog data converters interface to analog chips and RF ICs	Offers the flexibility and choice of multiple RFIC implementations
ARM AMBA On-Chip Bus Interconnect	AMBA 4 AXI, AMBA 3 AXI and AMBA 2 AHB/APB interconnects	Optimized IP for AXI interface compliant to AMBA Ordering Rules, enabling high performance and cache coherency

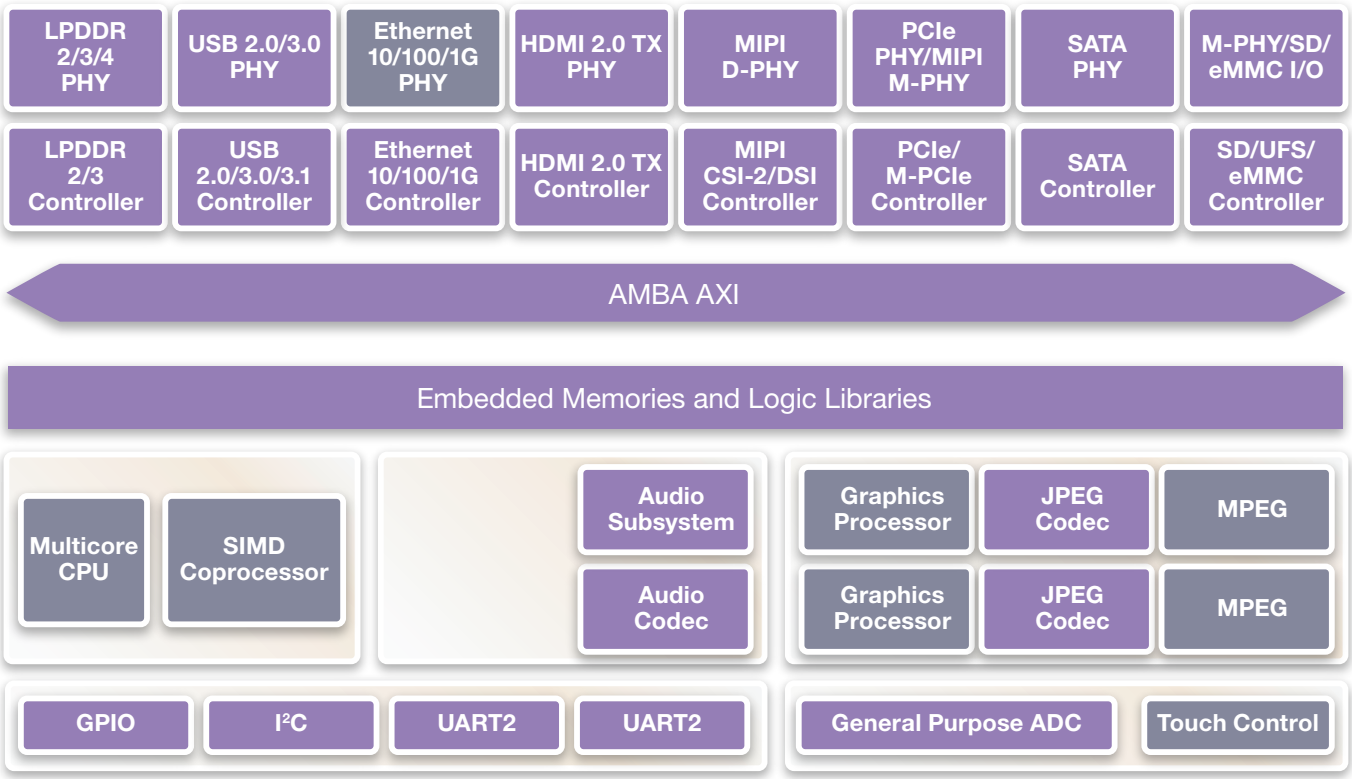

Figure 1: Typical Mobile SoC with DesignWare IP

Summary

There are certain trends that are very clear in the mobile market. Whether the goal is to provide new features, reduce power, or improve performance, Synopsys provides a broad portfolio of IP that is optimized for mobile applications that will help you achieve your design goals faster and with significantly less risk.

For more information on DesignWare IP mobile SoC designs, visit: www.synopsys.com/mobileIP

Sources

1. Pew Research Center: http://www.pewresearch.org/fact-tank/2013/06/06/cell-phone-ownership-hits-91-of-adults/
2. Gartner: http://www.gartner.com/newsroom/id/2954317
3. Forbes: http://www.forbes.com/sites/chuckjones/2014/11/27/china-mobiles-4g-explosive-growth-is-positive-for-apple/

SYNOPSYS® Accelerating Innovation

Synopsys, Inc. • 690 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

02/15.RP.CS5375.