With the increasing hardware and software complexity in today’s SoCs, companies need more from their IP providers to help meet their project schedules. Delivering IP blocks alone is no longer adequate to address the growing SoC design and integration challenges. Designers require solutions that ease IP configuration and integration into the overall SoC and accelerate their software development effort. The Synopsys IP Accelerated initiative redefines the IP supplier paradigm with solutions that address designers’ challenges with IP prototyping, software development and integration.

The IP Accelerated initiative consists of the following solutions:

- IP Prototyping Kits
- IP Virtual Development Kits
- IP Subsystems
Overview

Today, semiconductor companies are creating complex SoCs under significant time-to-market pressure. With the rise in software content as well as more IP (and more complex IP) being integrated, customers are faced with the challenge of not only quickly integrating the IP into the SoC, but also accelerating software development and SoC integration schedules. With this in mind, companies are requiring more from IP suppliers. Synopsys’ IP Accelerated initiative goes beyond the traditional IP supplier paradigm, redefining what is expected from IP providers to help designers achieve successful IP integration into SoCs with less effort, lower risk and faster time-to-market.

“Due to increasing design complexity, escalating design costs and shorter time-to-market, the percentage of third-party design IP usage is expected to more than double from 2012 to 2018. More companies are turning to third-party IP providers, such as Synopsys, to provide comprehensive solutions such as those defined in the IP Accelerated initiative to lower their development cost, reduce integration risk and meet their market schedules.”

– Richard Wawrzyniak, senior market analyst, ASIC and SoC at Semico Research Corporation

Synopsys’ IP Accelerated initiative augments Synopsys’ broad portfolio of silicon-proven DesignWare® IP with IP Prototyping Kits, IP Virtual Development Kits and IP subsystems to enable fast prototyping, software development and integration of IP into SoCs. Below are key highlights of the initiative:

- The DesignWare IP Prototyping Kits include a proven reference design for the IP preloaded onto a HAPS®-DX prototyping system and a software development platform running Linux® OS with reference drivers
- The DesignWare IP Virtual Development Kits are software development kits (SDKs) that include a processor subsystem reference design, a configurable model of the DesignWare IP as well as a Linux software stack and reference drivers
- For hardware engineers, the IP Prototyping Kits provide a validated IP configuration that can be easily modified to explore design tradeoffs for the target application
- For software developers, both the IP Virtual Development Kits and IP Prototyping Kits can be used as proven targets for early software bring-up, debug and test
- To reduce risk and accelerate time-to-market, Synopsys’ pre-verified Audio IP Subsystem, Sensor & Control IP Subsystem, and customizable Interface IP Subsystems deliver complete, complex functions that are ready to integrate into an SoC

Accelerating IP Bring-Up and Prototyping

The IP Accelerated initiative provides solutions that enable hardware engineers to quickly bring-up and prototype DesignWare IP. With the included proven reference design, ARC®-based software development platform running Linux OS and reference drivers, the DesignWare IP Prototyping Kits enable hardware engineers to develop an IP prototype in a matter of minutes versus weeks and immediately start implementing the IP in an SoC context.

DesignWare IP Prototyping Kits

The DesignWare IP Prototyping Kits center around a complete, out-of-the-box reference design that consists of a validated IP configuration and necessary SoC integration logic such as clock, reset, power management and test logic for a specific IP protocol, implemented on Synopsys’ HAPS-DX FPGA-based prototyping system. With a proven reference design for the IP, designers can be instantly productive, enabling them to accelerate the integration of IP into their target SoC, optimize the IP configuration and develop drivers and software applications with real world I/Os and hardware. The IP Prototyping Kits include a fast iteration flow that enables designers to modify the IP for the target application and explore design tradeoffs.

The IP Prototyping Kits include Synopsys’ HAPS-DX FPGA-based prototyping system that uses a Xilinx®-7 FPGA for capacity up to four million ASIC gates with a flexible I/O architecture to support both Synopsys HapsTrak 3 and industry standard FPGA Mezzanine Card (FMC) formats for real-world connections. The kits also include a PHY daughter board, simulation testbench and either a PC connection or a DesignWare ARC-based software development platform running Linux OS, Linux reference drivers and Linux applications examples. Designers can modify the standard IP configuration for the target application through a fast iteration flow, consisting of Synopsys’ coreConsultant IP configuration tool and Synopsys’ ProtoCompiler DX synthesis and debug tool, as well as compilation scripts. The IP Prototyping Kits can be extended to the full SoC by connecting the PHY’ daughter card to a Synopsys HAPS-70 FPGA-based prototyping system.

Figure 1: Synopsys’ DesignWare IP Prototyping Kit: Out-of-the-Box Solution
With the IP Prototyping Kit, designers only need to connect the HAPS-DX prototyping system to a PC or the ARC processor-based software development platform, insert the PHY daughter board, and plug in a keyboard and display to start optimizing the DesignWare IP configuration in minutes, develop drivers and software and use the reference designs to connect the IP to the SoC.

**Accelerating Software Development**

The IP Accelerated initiative provides software development kits (SDKs) that are either physical (IP Prototyping Kits) or virtual (IP Virtual Development Kits) targets for early software bring-up, debug and test concurrently with SoC development. Out-of-the-box support for a Linux software stack ensures that software developers are up and running instantly and can focus on the IP-specific software (e.g., drivers, bootcode, firmware). The SDKs can easily plug into existing software tool chains and interface seamlessly with the most popular embedded software debuggers, providing system-wide debug and analysis capabilities.

**DesignWare IP Virtual Development Kits**

Synopsys DesignWare IP Virtual Development Kits are SDKs that use a virtual prototype to enable developers to quickly bring-up, debug and test software for DesignWare IP in parallel with SoC development. The IP Virtual Development Kits consist of a reference virtual prototype, which includes a model of a multi-core ARM® Cortex® A-57 Versatile™ Express board and a configurable model of DesignWare IP.

"Due to the growing size and complexity of software, semiconductor companies are looking for solutions to help with the escalating cost and effort of embedded software development. With semiconductor companies now dedicating more than 50% of their development to software, DesignWare IP Virtual Development Kit will enable companies to stay competitive in an increasingly software-driven market."

– Chris Rommel, executive vice president of M2M and Embedded Technology at VDC Research

The IP Virtual Development Kits run Linaro® Linux with reference drivers for the DesignWare IP and provide non-intrusive debug control and visibility. In addition, its Eclipse-based tools interface seamlessly with the most popular embedded software debuggers such as Eclipse CDT, DDD, Lauterbach TRACE® and ARM DS-5. As the ARMv8 processor has both 64-bit and 32-bit operating modes, the DesignWare IP software can be optimized for the target mode and application. The reference IP Virtual Development Kits can easily be extended and modified to reflect the target SoC.

**IP Subsystems**

As both hardware and software complexity increases, more advanced and integrated IP solutions are required to help designers meet their aggressive project schedules without compromising quality. Synopsys’ pre-verified DesignWare Interface IP Subsystems, Audio IP Subsystem, and Sensor & Control IP Subsystem deliver complete, complex functions that are ready to integrate into an SoC.

By pre-integrating specific IP blocks together with an efficient processor and software in a single subsystem, Synopsys gives designers configurable, SoC-ready subsystem solutions that can significantly reduce their design and integration effort, lower design risk and accelerate time-to-market.

**Figure 3: DesignWare IP Virtual Development Kits Accelerate Software Development**

**Figure 4: IP Subsystem Integration Expertise**
Summary
As companies continue to face tremendous time-to-market pressures to stay competitive, the traditional IP supplier approach is no longer sufficient to meet their SoC development needs. To address the exploding software content and increasing complexity of SoC designs, Synopsys' IP Accelerated initiative redefines the IP supplier paradigm, providing DesignWare IP Prototyping Kits, DesignWare IP Virtual Development Kits and IP subsystems to help designers achieve faster IP prototyping, earlier software development, and easier IP integration.

For more information on Synopsys IP Accelerated initiative, please visit: synopsys.com/ip-accelerated