

SYNOPSYS®

# IP Accelerated

DesignWare IP, Tuned to Your SoC



# IP as Unique as Your SoC

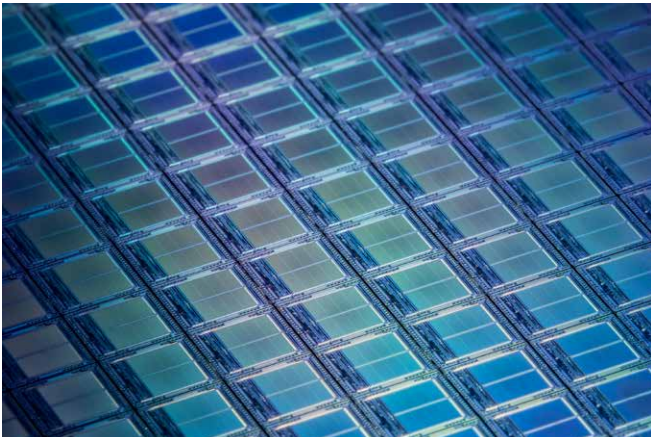
When building SoCs for your fast-paced markets, integrating IP that's tuned to your design will give you a competitive edge. Off-the-shelf IP alone is no longer enough to address your design challenges. Expect more from your IP provider, including solutions that ease IP configuration and integration and accelerate software development.

Synopsys' IP Accelerated initiative redefines what is expected from IP providers to help you successfully integrate IP into your SoCs with less effort, lower risk, and faster time-to-market.



## Get the SoC Architecture Right—From the Start

Every complex SoC design is created under significant time-to-market pressure. With the rise in software content as well as more IP (and more complex IP) being integrated, designers are faced with the challenge of meeting their performance, power and area targets without overdesigning their SoCs.



As part of your design team, Synopsys' SoC Architecture Design consultants will help you get your SoC off to the right start. They are ready to apply their expertise from years of designing mobile, automotive, networking and IoTs SoCs to your unique design. The consultants apply and share their deep knowledge in:

- CPU, DSP, and ASIP capabilities
- Establishing low power strategy
- Design of key blocks (RTL, ASIP)
- PPA estimation
- Memory architecture, bus bandwidth/latencies
- Verification and FPGA-based prototyping

*“The Synopsys team made detailed recommendations to test and bring up our AI SoC’s complex interfaces, helping ensure our on-schedule launch.”*

~R&D Director, Leading Artificial Intelligence Computing Company



## Pre-Verified IP Subsystems, Customizable by Your Team or Ours

As both hardware and software complexity increases, you need more advanced and integrated IP solutions to meet your aggressive project schedules without compromising quality. Whether you need a single controller and PHY integration, a combination of multiple protocols, or complete subsystems with processors and the software stack, Synopsys experts deliver IP subsystems tuned to your SoC.

Synopsys' configurable, pre-verified IP Subsystems deliver complete, complex functions that are ready to integrate into your SoC as-is, or be customized by your team or ours.

By integrating specific IP blocks together in a single subsystem, Synopsys provides you with another option to reduce your design and integration effort, lower design risk, and accelerate time-to-market.

## Smooth PHY Integration for High-Performance Designs

Your SoC's performance, floorplan, and pad ring requirements are unique, requiring customizable IP that meets your needs. While optimizing an implementation by hand can be challenging, as it involves analyzing and fine-tuning design parameters, Synopsys IP Hardening experts use an automated hardening flow to refine the implementation iteratively, for higher productivity and faster design completion.

For successful high-performance interfaces, designers need a well-controlled signal integrity and power integrity (SIPI) environment during the design and layout phase. Synopsys supports designers in creating such environments with tight skew control, optimum termination values, and clean reference levels, helping ensure that your signal and power integrity targets are met.

The signal integrity report service evaluates:

- On-chip decoupling capacitance
- Power and ground pins
- PHY & SDRAM termination strategy
- SoC package design
- PCB stack-up and trace width/spacing
- Performance at required data rate
- Read/write/address/command/control timing budgets

## 6 ways Synopsys supports your vision with our expertise:

1. Experienced SoC architecture consultants
2. Customizable, pre-built IP subsystems
3. Automated IP hardening flow
4. Structured signal & power integrity environment
5. Complete IP prototyping kits
6. On-site or remote silicon bring-up support

*“The combined hardening and SIPI consultation resulted in a gain of +32ps margin across the LPDDR4-3200 interface, and using the IP subsystem accelerated our overall design cycle.”*

~ASIC Design Director, Leading Mixed-Signal Semiconductor Company

## Accelerate IP Software Development, Prototyping and Integration

The DesignWare IP Prototyping Kits provide the essential hardware and software elements needed to reduce IP prototyping and integration effort to enable you to start implementing IP in a SoC in minutes.

With a proven reference design for the IP, designers can be instantly productive, enabling them to accelerate the integration of IP into their target SoC, optimize the IP configuration, and develop drivers and software applications with real world I/Os and hardware. Designers can modify the standard IP configuration for their target application through a fast iteration flow consisting of Synopsys' coreConsultant IP configuration tool, Synopsys' ProtoCompiler DX synthesis and debug tool and compilation scripts.



### Hardware/Software Options

IP Prototyping Kits come in multiple hardware/software configurations to meet your exact IP prototyping needs. The target IP core can be implemented on a Synopsys HAPS® FPGA-based prototyping system with an ARC® processor-based 32-bit software development platform (SDP) running Linux or a PCI Express connection to a PC with any processor. For designers who are already using HAPS systems, IP Prototyping Kits are available as soft deliverables that are compatible with their existing systems. All kits include reference drivers, SoC integration logic, and application examples.



### Ensure High Quality, Ready for Mass Production

Every project has unique requirements, and your IP test plan needs to align. Synopsys' silicon bring-up support team helps you design and track your IP subsystem test while sharing their in-depth knowledge of the IP, either remotely or during on-site support from one of our worldwide R&D sites.

Synopsys' design and IP experts will work closely with your team to review the test design and implementation, logic integration, timing, layout, package design, and PCB design, all with the shared goal of silicon success.

## About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes [logic libraries](#), [embedded memories](#), [embedded test](#), [analog IP](#), [wired and wireless interface IP](#), [security IP](#), [embedded processors](#), and [subsystems](#). To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' [IP Accelerated initiative](#) offers [IP prototyping kits](#), IP software development kits, and [IP subsystems](#). Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit [synopsys.com/designware](https://www.synopsys.com/designware).