

DesignWare Library

AMBA IP with coreAssembler

Overview

The power of DesignWare® Library intellectual property (IP) with coreAssembler technology enables you to create, simulate, and synthesize AMBA™-based subsystems in less time than ever before. DesignWare Library IP with coreAssembler uses assembly technology targeted at both AMBA 3 AXI™ and AMBA 2 AHB/APB™ subsystems to automate design creation and initial subsystem validation, reducing the time spent creating AMBA protocol-based application platforms.

Benefits

- Reduces time to first simulation from weeks to hours
- Reduces time to first placed gate from months to days
- Proven IP interoperability
- Built-in design expertise lets you focus on your design differentiation

Features

- Automated assembly of DesignWare Library AMBA 3 AXI and AMBA 2 AHB/APB synthesizable IP components
- Supports AMBA 3 AXI and AMBA 2 single, multi-layer, and AMBA-Lite™ configurations
- System-level configuration with parameter propagation
- Automated address map generation
- 3rd party IP integration support (requires additional coreAssembler license)
- Built in verification expertise
 - Automated initial testbench infrastructure generation
 - Automated block-level verification
 - Automated subsystem-level verification

- Automatic instantiation of DesignWare Verification IP components for AMBA 3 AXI and AMBA 2 AHB/APB
- Automated stimuli generation¹
- Expert-level simulation, synthesis, test and formal scripts automatically generated

Reducing the time to first simulation and time to first placed gates significantly reduces the overall design cycle. Initial design of an AMBA-based subsystem requires many steps that are crucial but that do not differentiate the application. These tasks include:

- Writing an RTL module for selected IP ensuring they are connected correctly
- Creating the memory address map for the subsystem
- Writing an initial testbench and stimuli to verify the subsystem connections
- Creating simulation and synthesis scripts

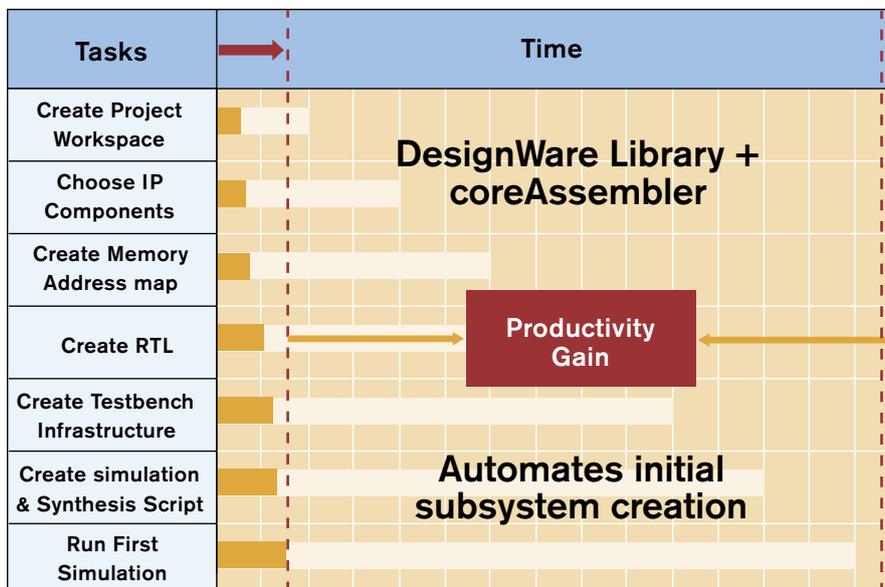


Figure 1: Reducing the time to first simulation with DesignWare Library IP and coreAssembler.

RTL module-to-module wiring errors can be made while manually connecting hundreds of pins together. These wiring issues, while typically are simple editor mistakes, are time intensive to debug and correct. Creating the memory address map is a complex task, but without an accurate map, the subsystem will not be able to function even at the simplest level. The quicker the testbench, stimuli and scripts are created, the quicker the subsystem verification task can be started.

DesignWare Library IP with coreAssembler technology automates the flow of subsystem assembly, simulation and synthesis, therefore significantly reducing the engineering effort required to design AMBA-based subsystems. Any AMBA 3 AXI or AMBA 2 AHB/APB, single or multi-layer subsystem configuration is supported, in addition to AMBA-Lite configurations. With the automation of these steps, configuration errors are eliminated and designers are free to focus on application specific tasks.

The flow includes an automatically created memory address map and creation of the initial subsystem testbench. The subsystem testbench has the option to include a set of generated tests to check that the subsystem can be accessed. The generated AMBA transactions are executed by the DesignWare Verification IP components. These verification tasks can be quickly modified to increase the overall bus coverage. The DesignWare Verification IP monitors are used to track protocol coverage and provide notification of any protocol violations.

Subsystem Creation

With DesignWare Library IP and coreAssembler, the creation of new subsystems is simple. You can add/remove subsystem components, export interface signals, change connections, re-name ports, configure the subsystem, configure individual components, and generate a full memory address map for the system. All of the DesignWare Library synthesizable IP components support the knowledge-based flow.

Summary

DesignWare Library IP with coreAssembler is the only cohesive environment to offer knowledge-based assembly with an available range of implementation and verification IP for an AMBA-based subsystem. The automated knowledge-based assembly eases subsystem creation taking the guesswork out of IP integration and providing guaranteed IP interoperability. DesignWare Library IP with coreAssembler substantially reduces subsystem design time and cost. Time to first simulation is reduced from weeks to hours. Time to first placed gate is reduced from months to days. The standardization of the IP integration flow means that subsystems created with DesignWare Library IP and coreAssembler can be easily reused in subsequent projects.

When coreAssembler is used with the DesignWare Library IP the coreAssembler automated assembly features are licensed by the standard DesignWare Library license. Additional coreAssembler features, such as SPIRIT import and template export, require a full-featured coreAssembler license.

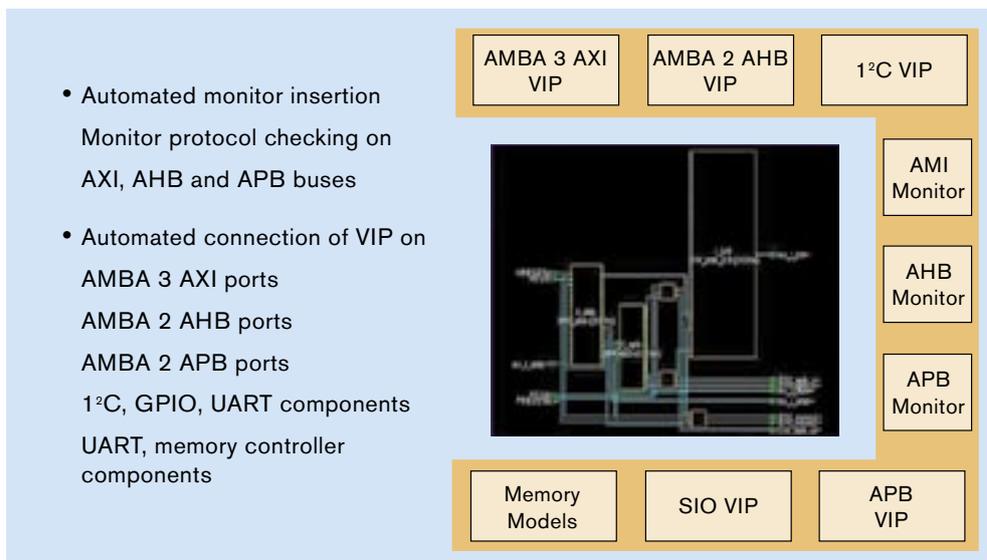


Figure 2: Automated initial testbench with DesignWare Verification.

About DesignWare Library

Synopsys DesignWare IP enables designers to quickly create and verify complex SoCs, ASICs and FPGAs. DesignWare IP, when combined with Synopsys' robust IP development methodology, extensive investment in quality and comprehensive worldwide technical support, gives designers a faster, more predictable and lower risk path to chip success. The DesignWare Library portfolio includes foundry libraries, verification IP, AMBA bus IP and peripherals, memories, building block IP and microcontrollers. All are available under one license with no additional costs, per use fees, or royalties.

**For more information on DesignWare IP, visit:
www.designware.com.**

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700 East Middlefield Road, Mountain View, CA 94043 www.synopsys.com

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