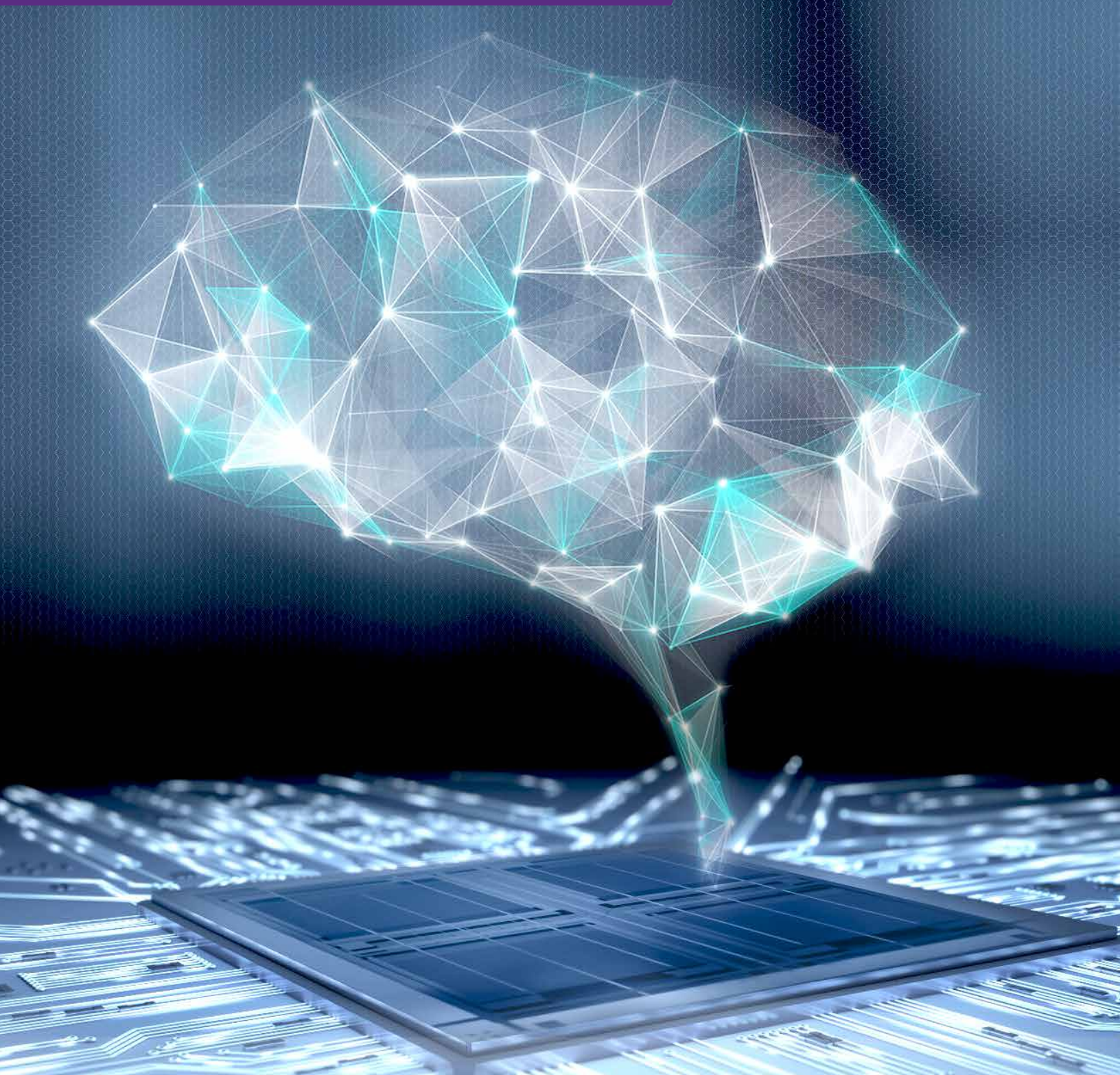
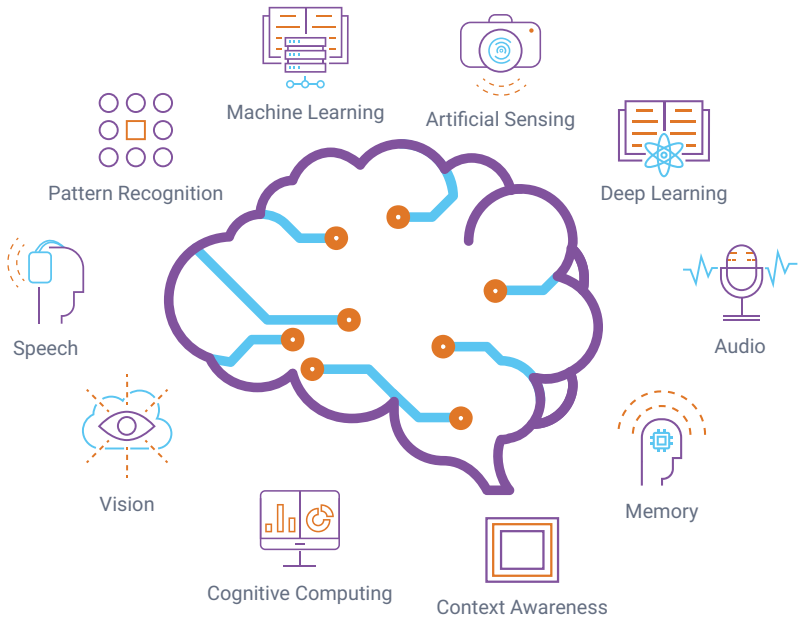
SYNOPSYS®

DesignWare IP for Artificial Intelligence



The recent innovations in deep learning algorithms and neural network processing is driving new technology requirements for artificial intelligence (AI) SoCs. Deep learning capabilities are being added to SoCs across all markets including mobile, IoT, data center, automotive, and digital home. Synopsys' silicon-proven DesignWare® IP portfolio is addressing the diverse processing, memory, and connectivity requirements of each market.



Artificial intelligence capabilities

Deep Learning SoC Design Challenges

Specialized processing is required to manage massive and changing compute intensities for machine and deep learning tasks. Memory performance becomes a critical design consideration to support new complex artificial intelligence models. Capacity and bandwidth are primary concerns for training, while inference optimizations create irregular memory access challenges. Real-time data connectivity between sensors, such as CMOS image sensors for vision, and deep learning accelerators become key components. Power consumption is reduced by minimizing data movement between the processor and memory, using key power management features, and designing in advanced FinFET technologies.

Benefits of DesignWare IP for Deep Learning

Specialized Processing

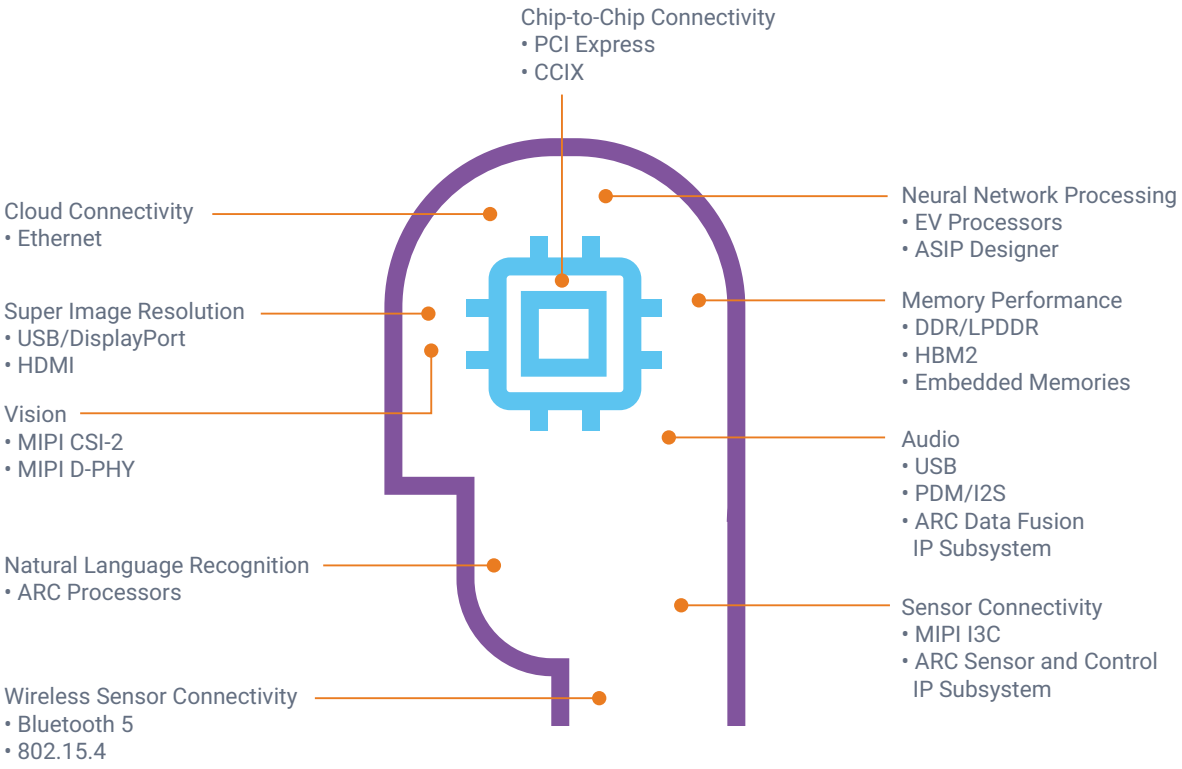
Synopsys provides a portfolio of embedded processors to efficiently execute the varied workloads of AI applications. This includes IP and tools for scalar, vector, and neural network processing. The ARC® EV Processors integrate heterogeneous computing elements optimized for embedded vision applications, including convolutional neural networks (CNNs). The ARC HS and EM Processors combine RISC and DSP processing capabilities to deliver the best balance of performance, power, and area. ARC's extensible instruction set architecture enables users to add their own instructions or hardware to accelerate AI algorithms and tightly couple memories and peripherals to the processor to reduce system bottlenecks. For custom AI workloads that benefit from a high degree of parallelism and specialized datapath elements, Synopsys' ASIP Designer tool automates the development of custom processors and hardware accelerators.

Memory Performance

Synopsys provides memory IP solutions to support efficient architectures for different AI memory constraints: bandwidth, capacity, cache coherency. The latest DDR IP addresses capacity needs for data center AI SoCs. HBM2 IP addresses the bandwidth bottleneck while providing an optimized off-chip picojoules (pJ) per bit memory access. CCIX IP enables cache coherency with virtualized memory capabilities for AI heterogeneous compute and reduced latency in AI applications. A wide array of embedded memory compilers enable high density, low leakage, and high performance on-chip SRAMs options including, TCAMs, and multi-port memories.

Real-Time Data Connectivity

Synopsys provides reliable connectivity to CMOS image sensors, microphones, and motion sensors for AI applications including vision, natural language understanding, and context awareness. The interface IP portfolio in advanced FinFET process technologies reduce power and support a range of widely used standard specifications like MIPI, USB/DisplayPort, HDMI, PCI Express, Cache Coherent Interconnect for Accelerators (CCIX), Ethernet, and more.



DesignWare IP for artificial intelligence designs

	DesignWare IP for Specialized Processing
Embedded Vision Processors	Verified embedded vision solution including the scalar, vector DSP, and high performance CNN engine and a suite of software tools supporting frameworks and mapping tools for AI model optimizations
ARC Processors	Scalar and vector processing capabilities with APEX extensions, combined with tightly coupled memories for AI acceleration and addressing the key deep learning bottlenecks
ASIP Designer	Industry-leading tool to design your own scalar, vector, and deep learning processors; deploys hardware parallelism & custom datapaths while retaining programmability
Foundation Cores	Math operations including dot product form the building blocks of specialized AI processor designs

	DesignWare IP for Memory Performance
LPDDR4/4x	Supports the latest LPDDR4/4x and future LPDDR5 standards, enabling the lowest interface voltage for low power AI inference
DDR4	Maximum available capacity for AI training; supports the latest DDR specification
HBM2	High Bandwidth capabilities with optimized off-chip pJ/bit memory access address the critical bottleneck of data center AI SoCs
CCIX	Cache coherency and virtualized memory capabilities enable AI heterogeneous compute and reduced latency; Flexible interface support for easy integration with Arm-based, 3rd party, or customer's own coherent fabrics
Embedded Memories and Logic Libraries	Efficient on-chip memory configurations via a wide array of embedded memories, TCAMs, logic libraries, and multi-port memory solutions optimized for AI applications; near threshold voltage options reduce power, and design analysis enables large SRAM arrays for maximizing local memory

	DesignWare IP for Real-Time Data Connectivity
PCI Express 5.0	High speed capabilities enable AI accelerators that are configurable, optimized, and ready for plug and play interconnect; supports all the latest PCIe features including 32GT/s for maximum performance
MIPI CSI-2	Complete camera solution for machine vision; support for multiple image pixel interfaces to merge multiple streams; 1 to 8 RX data lanes with D-PHY Protocol Interface (PPI)
MIPI D-PHY	Direct CMOS image sensor connectivity; supports v1.2 specification at 2.5Gbps/lane; available in wide range of processes including FinFET
MIPI I3C	Multiple sensor integration for context awareness or other deep learning applications; backward compatible with the I2C slave devices at data rates up to 33.4 Mbps; supports master or slave configurations
USB/DisplayPort USB Type-C	Connectivity for all video markets in mobile, digital TV, set-top box, cameras, and more for image super resolution; supports audio bursting, lowering power consumption for microphone & speaker connectivity for AI
HDMI 2.1	Complete RX/TX solution; supports uncompressed 8K resolutions
Bluetooth 5/802.15.4	Wireless sensor connectivity including Bluetooth low energy's new AoA, AoD features
Ethernet	Comprehensive portfolio for 10M through 100G Ethernet applications; supports the latest IEEE specifications, including Time Sensitive Networking (TSN), Audio Video Bridging (AVB) and offloading features

	DesignWare ARC Subsystems for Specialized Processing, Memory Performance, and Real-Time Data Connectivity
ARC Sensor and Control IP Subsystem	Pre-validated, tightly integrated (memories & peripherals) subsystem for significant power savings with AI-specific hardware accelerators (i.e. sensor fusion, motor control)
ARC Data Fusion IP Subsystem	Efficient, low-power solution for AI triggering functions including voice & gesture recognition, face detection; tightly coupled PDM and I2S peripherals simplify integration of external audio devices; audio processing libraries provide building blocks for AI audio applications
ARC Secure IP Subsystem	Solution for protecting high value targets against wide variety of malicious attacks; high performance cryptography protects AI communications with the cloud; anti-tamper features protect AI edge devices from local attacks

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.

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