Overview
Embedded memory is being implemented in more than 30 percent of all designs today\(^1\) and is taking up more and more die area. While embedded memory presents significant system performance and cost reduction advantages, it also brings its own testing issues. Test vector style tests are not suitable for verifying embedded memory arrays. It’s too costly, because the time spent in the manufacturing tester grows exponentially as the embedded memory die area increases. Sometimes it is impossible to create a set of vectors that can detect all possible types of memory defects.

These problems can be alleviated by implementing embedded memory built in self-test (BIST). In simplistic terms, memory BIST is an on-chip utility that enables the execution of a proven set of algorithmic style verification tests directly on the memory array. These tests can be executed at the design’s full operating frequency to prove the memory array operations and identify errors caused by silicon defects.

The DesignWare\textsuperscript{®} Memory BIST MacroCell, DW\textsubscript{rambist}, is a configurable, fully synthesizable solution for memory built-in self test of embedded SRAM memory structures. DW\textsubscript{rambist} increases overall product quality by ensuring fault coverage of embedded memory defects through built-in algorithmic testing. In order to reduce test time and maximize utilization of embedded test resources, DW\textsubscript{rambist} executes tests in parallel with a shared BIST controller. Four industry-standard SRAM BIST algorithms are selectable at runtime: March LR, March C-, MATS++, and a retention test using a pause-polling mechanism.

\(^1\) Gartner Dataquest End User Analysis, System Designers’ Wants and Needs, Dec 25 2001
High-Performance System Support with Tightly Coupled Memories

Performance is an important requirement for systems that include embedded memory. The timing overhead of a mux cell on the critical data path is not acceptable, because the mux delay would seriously affect the overall system performance. The DW_rambist solves this problem with a pipelining feature. Users have the option to insert pipeline stages on the data path, thus maintaining high-speed operation of the overall system and tightly coupled memories.

Error Diagnostics and Support for Repairable Memories

During power-on or reset testing, the DW_rambist MacroCell can be configured to produce a simple pass or fail flag. Failing addresses and data can subsequently be scanned out during manufacturing tests and used to diagnose the type of failure. The designer can then assess if the memory can be corrected with the memory vendor’s repair techniques.

Integrating the DW_rambist MacroCell into your design

Like all DesignWare MacroCells, DW_rambist is delivered together with Synopsys’ coreConsultant tool, which automates installation, configuration, simulation and synthesis. Using coreConsultant, the user enters specific memory design information (e.g. type and size) and selects which BIST algorithms he wishes to run. The memory description may also be entered via an ASCII text file that enables automated generation of the memory wrappers and connections. coreConsultant then automatically generates the synthesis scripts and sample test scripts to drive scan chain insertion, ATPG with Design Compiler™ and TAP insertion with BSD Compiler.
Summary of DW_rambist MacroCell Features

- Interfaces
  - IEEE 1149.1 TAP controller interface
  - Two clock interface, one for TAP I/F, second for at-speed BIST execution

- Error Diagnostics
  - Pause on first and subsequent failures mode, serial debugging
  - Failing address and data may be scanned out for examination
  - Quick debug mode, continue on failures mode, failing addresses not recorded
  - Parallel debug port to observe the failing memory data bits

- BIST Tests
  - User choice of March LR (14n), March C- (10n) and MATS++ (6n)
  - Custom (user defined) patterns option

- Optional SRAM retention test, (5n + delay), auto pause mechanism
- Selection of background and complement background data patterns
- Default sequence or run time selection of individual test

- Supported Memories
  - Synchronous and asynchronous SRAM
  - Pipelining support
  - Support for 32 memories per BIST controller
  - Highly configurable memory interface to suit most types of memories

- Supported Memory Configurations
  - True at speed testing of memories in parallel
  - Memory array test via single-port and multi-port

- Ability to enable/disable testing of individual memories
- Multiple controller scheduling
- Support for incomplete address space

- Design for Test
  - Configurable shadow logic capture
  - Sample script for scan chain creation and connection
  - Integration with DFT Compiler, BSD Compiler and TetraMAX®

For more information about Synopsys products, support services or training, visit us on the web at www.synopsys.com, contact your local sales representative or call 650.584.5000.