Data Sheet

SYNOPSYS®

DesignWare Library 6811 MacroCell

Overview

The DesignWare® 6811 MacroCell (DW_6811) is a high-performance, synthesizable and configurable 8-bit microcontroller designed for fast and easy integration into SoC, ASIC, or FPGA designs. The technology-independent DW_6811 MacroCell is fully binary compatible with the industry standard 6811 microcontrollers and includes a complete verification environment. To ensure ease of use, this powerful solution is packaged with Synopsys' coreConsultant tool, a user-friendly wizard, which walks the designer through the necessary steps of core integration, including configuration, simulation, and synthesis.

To assure designers have access to the highest quality, reusable IP, the DW_6811 MacroCell has been developed according to the Reuse Methodology Manual (RMM), the defacto industry standard for reusable design methodologies. In addition, the DW_6811 MacroCell has undergone extensive testing during the design process and has been proven in many different technologies. This solution is ideal for building low-cost, high-performance embedded control systems.

Technical Highlights

- Implements standard 6811 architecture
  - Implements full M68HC11 instruction set
  - 4 clocks per instruction cycle
  - Special 16-Bit ALU arithmetic operations
  - Shared 64K byte code/data memory space
  - Dual 8-bit accumulators can be concatenated into double accumulator
  - Dual 16-bit index registers
- Power saving STOP and WAIT modes
- Bus Interface Unit (BIU) supports:
  - Internal RAM (256, 512, or 1K bytes)
  - Internal ROM (up to 64K bytes)
  - External RAM/ROM
  - SFR bus for custom peripherals
- 3 external reset/interrupt sources
- 17 internal interrupt sources

Included Peripheral Options

- 16-bit timer
  - Three Input Capture (IC) channels
  - Four Output Compare (OC) channels
  - One software selectable IC or OC channel
- 8-bit pulse accumulator
- COP watchdog timer system
- SPI synchronous serial port, basic or enhanced (SPI or SPI+)
- SCI UART, basic or enhanced (SCI or SCI+)

All of the above peripherals can be automatically added or deleted to meet the application needs.

High Performance Architecture

The DW_6811 core (shown in Figure 1) is a fully synchronous design, occupying between 15K and 30K gates depending on the speed, configuration and target technology. The optional math coprocessor will allow significant speed improvements for certain types of computations. The DW_6811 is designed for applications running at clock frequencies up to 200MHz (at 0.13µm), exceeding the performance available from off-the-shelf M68HC11 devices.

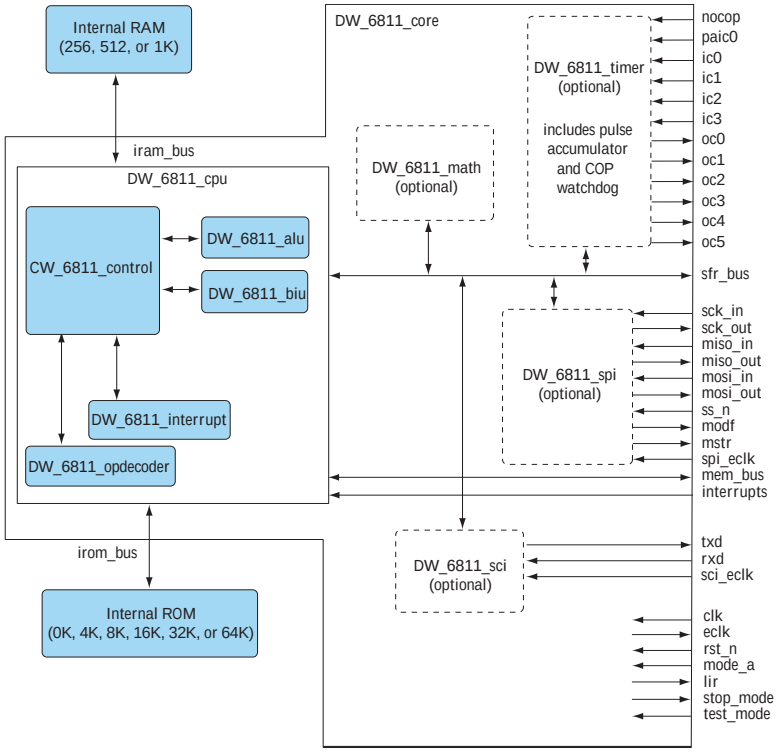

Figure 1: DW_6811 MacroCell Block Diagram

68HC11 Compatibility

The DW_6811 is object code compatible with the standard M68HC11 microcontroller family, and features the same rich instruction set contained in M68HC11 devices. In addition, it includes many of the standard peripheral functions found within the different M68HC11 device families. Each of the optional peripherals can be added or removed by the user during the core configuration.

Parameterized implementation of the DW_6811 peripherals enables users to customize the synthesized logic for their target applications. In addition, custom peripherals can be implemented by the user and easily interfaced via the special function register (SFR) bus.

Complete Set of Deliverables

The DW_6811 MacroCell solution includes the following deliverables:

- Multiple-simulator support (e.g., VCS™, Verilog-XL, NC-Verilog, MTI ModelSim-Verilog)
- An example M68HC11-compatible design
- Extensive verification environment
- Automatic installation, configuration, simulation, and synthesis with coreConsultant
- Complete documentation – DW_6811 databook and application notes in PDF format, integrated into the coreConsultant on-line help

About DesignWare IP

Synopsys' industry leading, high-quality DesignWare IP enables designers to create and verify innovative, cost-effective SoCs, ASICs and FPGAs. The broad portfolio includes industry leading connectivity IP Cores and Verification IP (e.g., USB 1.1, USB 2.0, USB 2.0 PHY, USB 2.0 On-The-Go, PCI, PCI-X, PCI Express, Ethernet, I2C), AMBA™ on-chip bus (logic, peripherals, verification IP) complete memory solution (e.g., memory controllers, BIST and models), high-speed datapath components, microcontrollers (8051, 6811) and Star IP processors and DSP core (e.g., IBM PowerPC(R); 440, Infineon C166™S and TriCore™1, MIPS32™ 4KE™, NEC V850E™, Philips CoolFlux™ DSP). When combined with our robust IP development methodology, extensive investment in quality and comprehensive worldwide technical support, DesignWare IP gives designers a fast, predictable and low-risk path to chip success.

The encrypted version of the DesignWare 6811 MacroCell is included in the DesignWare Library at no additional cost. The Source RTL of the DesignWare 6811 MacroCell can also be licensed individually, on a per-use basis.

For more information on DesignWare IP, visit www.synopsys.com/designware

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