In-Chip PVT Monitoring and Sensing

Highlights

- Distributed PVT Sensing Fabric
- Temperature profiling of SoCs
- Configurable by application
- Power optimization support
- Device reliability enhancement

Target Applications

- Data Center, AI, Automotive, 5G and Consumer
- Thermal mapping for workload balancing
- Optimization schemes DVFS, AVS, DFS, SVS
- Lifecycle management and design enhancement

Technology

- Sensor fabric with central controller
- Standard digital interfacing
- Advanced node and FinFET SoCs
- 28nm down to 3nm

Overview

Process, Voltage and Temperature (PVT) monitoring is critical to achieving successful operation and compelling performance of advanced node and FinFET semiconductor devices. Increasing transistor density and routing complexity presents several major challenges to the in-chip management of dynamically changing physical conditions during in-field operation, and in the way devices are manufactured and tested.

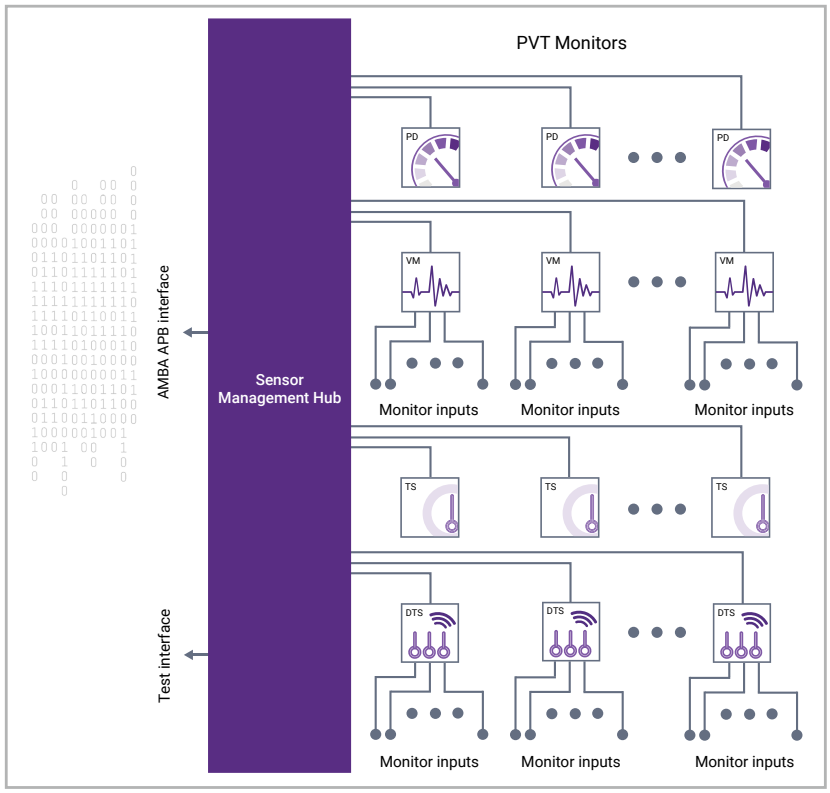

Figure 1: PVT Monitoring Subsystem

Unique Sensing Solution

Belonging to the Silicon Lifecycle Management (SLM) platform, the embedded monitoring and sensing technology from Synopsys offers a high accuracy, highly featured and well-supported monitoring solution to SoC designs from 28nm down to 3nm.

Sensor Management Hub (SMH)

The distributed subsystem solution consists of a range of sensors communicating to a central controller (or hub). Configurable by application, the subsystem is easily integrated with digital interfacing into the design-flow and architecture of the chip. Developed with digital design, production test development and software design teams in mind, the monitoring solution connects in to an SoC architecture via standard interfaces for normal and test phase operation. The flexible monitoring subsystem accommodates the evolving landscape of extended sensor products designed to measure in-chip conditions continuously throughout a silicon chip's lifetime, from fabrication to end-of-life. The range of sensors provides valuable data which enables powerful analytics algorithms to optimize device performance, enhance reliability and allow for predictive maintenance and failure.

Embedded Thermal Sensing

Thermal sensing within semiconductor devices today is a critical component in order to provide reliable, power-efficient and speed-optimized chip designs. SoCs on advanced FinFET nodes typically have high gate densities and therefore, power densities. Complex software driven workloads, multi-core and multi-accelerator architectures contribute to localized heating across the die which is difficult to manage and predict. Thermal sensing solutions available from Synopsys offer the following:

Benefits

- Distributed, high accuracy, low-latency, real-time thermal mapping of the die
- Enables support of DVFS and AVS schemes driven by precise thermal management
- Lifetime thermal stress analysis, supporting increased chip reliability

Use Cases

- **Data Center**—Hyperscale Data Centers with confidence, utilizing high accuracy thermal management, reducing electricity and operational overhead costs
- **AI**—Thermal monitoring of multi-core architectures, allowing tight thermal guard-banding to increase core/accelerator utilization
- **Automotive**—Enhanced thermal visibility enabling lifetime assessment, enhanced reliability, predictive maintenance and predictive failure
- **5G and Consumer**—Thermal aware solutions for increased power efficiency and extended battery up time. Longer product operation with improved user experience

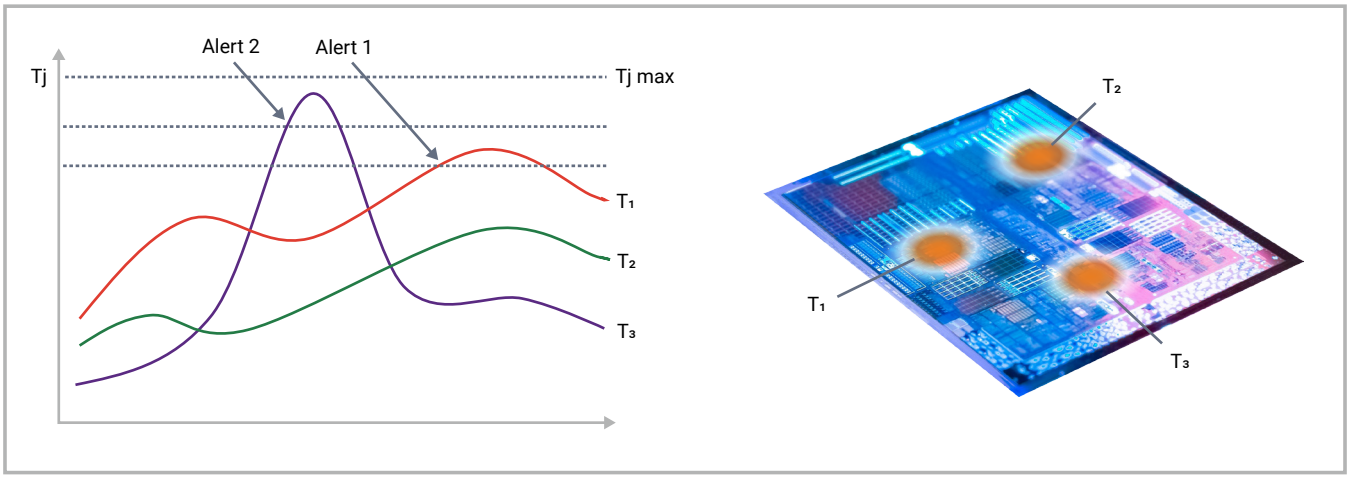

Figure 2: Localized thermal mapping and real-time tracking across the die

Supply Domain Monitoring

Healthy logic operation within advanced node devices is dependent on a sufficient supply being available. Compelling products are power optimized in order to enrich user experiences. The Voltage Monitor IP from Synopsys addresses this delicate balance by providing highly accurate, real-time core and IO supply monitoring throughout the chip.

Benefits

- Highly accurate voltage IR drop analysis
- Real-time, multi-point embedded supply monitoring
- Support for adaptive voltage supply (AVS) optimization schemes

Use Cases

- **Device Assessment in Production**—Screening of supply levels during production test, allowing for device binning by application or evaluation of chip power/speed performance profiles
- **Supply Droop Mitigation**—Detection of supply droop under heavy processor workloads
- **Power Optimization**—In-field optimization of supplies, supporting PMIC and regulator control loops

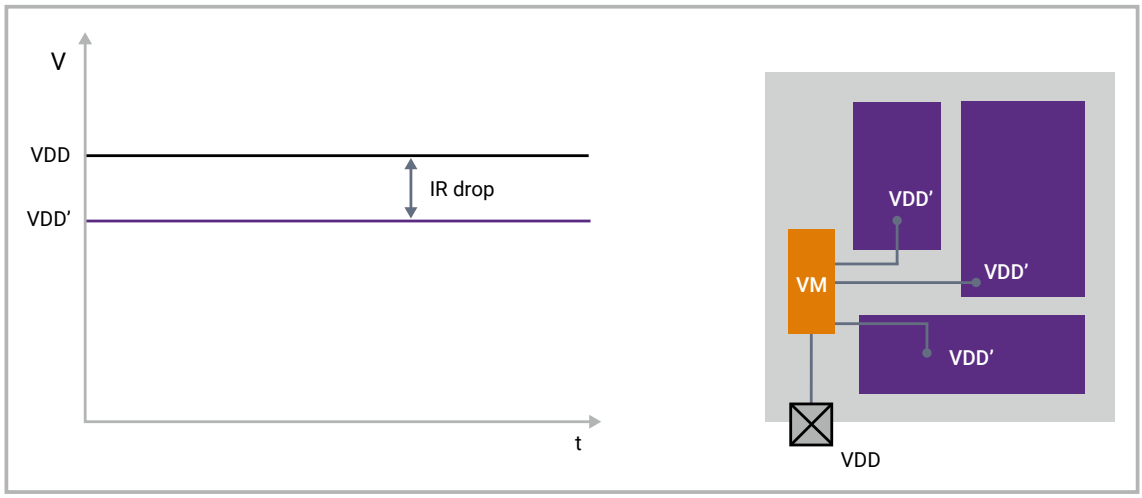

Figure 3: Multi-point voltage supply monitoring for IR drop analysis

Silicon Speed Detection

As silicon technologies scale, understanding the increasing process variability of transistor, logic and interconnect presents an opportunity for intelligent device assessment and selection. The Process Detector IP under-pins device screening, age monitoring and tracking of real-time circuit speed performance.

Benefits

- In-line, in-test and in-field production variability analysis of metal and gate loaded delay chain circuits, providing circuit delay assessment for power/speed optimization
- Small-scale solution for measurement of process variability at multiple points across the die, allowing for local and global variation assessment
- Enables measurement of thin and thick oxide transistor measurement for various transistor types
- Support of delay chain configurations consisting of customer-specified logic cells

Use Cases

- **Production Test**—Device assessment during production test for binning, power profiling and spread analysis
- **In-Field Aging**—Age and degradation monitoring during HTOL and in-field
- **Device Optimization**—Critical path delay assessment for power and speed optimization, supporting Dynamic Frequency Scaling (DFS) schemes
- **Device Normalization**—Supply adjusted devices depending on process corner

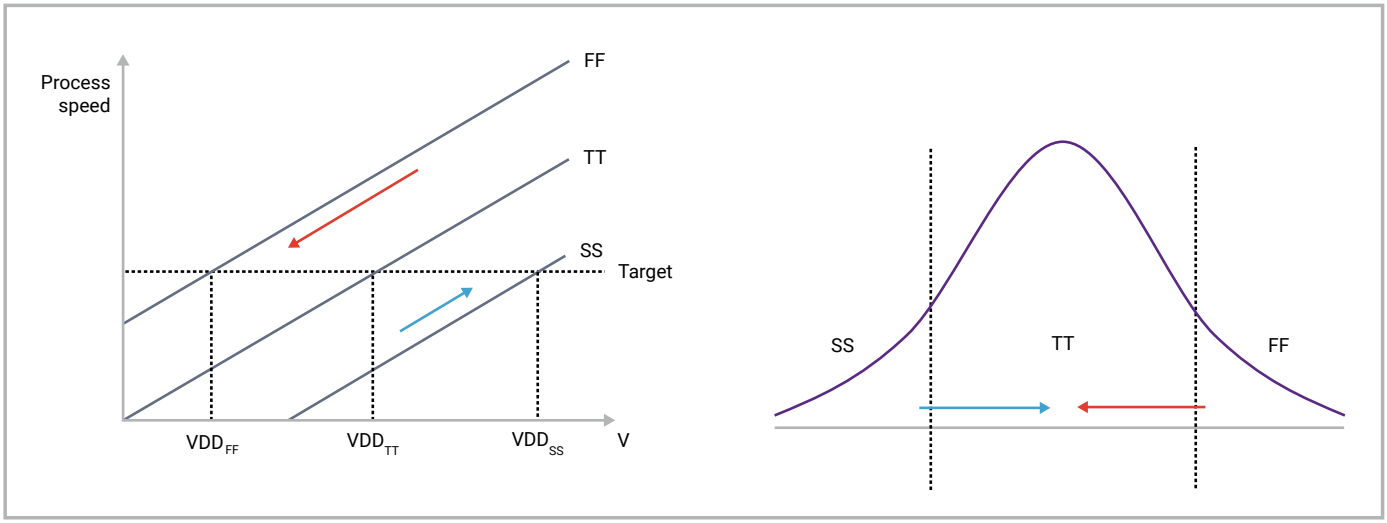

Figure 4: Supply adjusted devices through normalization based on silicon speed type

IP Features

- Application specific subsystem configuration
- Alerts, alarms and trigger conditions for safer, more reliable chip operation
- Internal self-checking for sensor health status management providing operational reassurance
- Digital interfacing for ease of integration and reliable sensor communications
- Standard interfacing, including AMBA APB for normal operation and iJTAG (compatible) test access support
- Scan-path enabled for high testability

PVT Monitoring Expertise and Support

- Monitoring IP has been developed by our expert engineering team since 2010
- Easy IP integration with extensive support documentation and application notes
- Production test results interpretation support

Integration Guidance and Placement

- Expertise provided in monitor placement and configuration, based on end-use application
- Optional floorplan layout review provided to assist with monitor and sensor placement

Deliverables

A comprehensive set of front-end and back-views are delivered to ensure ease of integration.

Documentation

- Datasheets, Application Notes and User Guides

Front-End (FE) Views

- LEF
- Verilog Model
- Liberty timing files

Back-End (BE) Views

- GDS Collateral (including tag and layer summary)
- DFT
- DRC Report (including antenna report)
- LVS Report (including ERC report)
- Netlist (for LVS purposes only)

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.

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