DesignWare Processor IP Portfolio

• Scalable family of 32-bit processor cores, vision processors, and subsystems
• Maximum power and area efficiency (DMIPS/mW, DMIPS/mm²) for embedded applications
• Highly configurable so each instance can be optimized
• Extensible instruction set enables application-specific customizations
• Integrated tool suite with broad hardware and software ecosystem support
DesignWare Processor IP Portfolio

**EM Family**
- Ultra-low power embedded processing
- Optimized for ultra-low power
- 3-stage pipeline RISC processors with RISC + DSP
- Maximum performance and area-efficiency: up to 1.81 DMIPS/MHz and as small as 0.01mm²

**SEM Family**
- Security processors for embedded applications
- Power- and area-efficient security processors for IoT and mobile applications
- Protection against hardware, software and side channel attacks
- SecureShield for Trusted Execution Environments

**HS Family**
- High-performance control
- Highest performance ARC cores
- Single or dual issue
- High-speed 10-stage pipeline, SMP Linux support
- Single-, dual-, quad-core configurations

**VPX Family**
- High-performance digital signal processing
- VLIW/SIMD architecture for highly parallel processing
- Multiple vector floating point engines
- Acceleration for linear algebra and complex math functions
- Optimized MLI running on DSP processor

**EV Family**
- AI-enabled embedded vision
- Multicore design optimized for vision processing
- High-performance vision engine can be configured for 8-, 16-, or 32-bit operations
- Programmable deep neural network engine with up to 14,080 MACs
- AES encryption protects valuable data from evolving threats

**Functional Safety Processor Portfolio**
- Support for ARC EM, HS, VPX, and EV Processor Families
- Integrated hardware safety features to detect system errors
- Acceleration of ISO 26262 certification for safety-critical automotive SoCs

Processor IP

Synopsys’ processor IP portfolio includes the DesignWare® ARC® processors and subsystems, software, development systems and tools. ARC processor cores are based on a flexible and proven 32-bit instruction set architecture (ISA) with features optimized for a broad range of embedded and deeply embedded applications:

- Performance-efficient designs deliver maximum performance while consuming a minimum amount of power and silicon area
- Highly configurable processors can be performance- and power-optimized for each instance on an SoC while sharing a common programming model
- Extensible ISA supports user-defined custom instructions, enabling integration of users’ proprietary hardware to accelerate application-specific tasks
- Streamlined system integration through the ability to closely couple memory and directly map peripherals to the core, reducing system latency and cost

**ARC EM Processors**

The ARC EM Family includes the ARCv2 ISA-based ARC EM4 and EM6 as well as the DSP-enhanced EM5D, EM7D, EM9D and EM11D. The ARC EM4, EM5D and EM9D processors support instruction and data CCMs and the EM6, EM7D and EM11D additionally support instruction and data caches. The EM9D and EM11D feature support for XY memories to deliver higher levels of signal processing efficiency. The ultra-compact EM cores feature excellent code density, small size and very low power consumption, making them ideal for power-critical and area-sensitive embedded and deeply embedded applications.

Along with optional FPU, MPU, µDMA, Real-Time Trace and ARConnet for multicore integration, the EM Family also offers an Enhanced Security Package, which provides tamper protection features and enables designers to create a trusted execution environment that protects their systems and software from evolving security threats such as IP theft and intentional remote attacks. In addition, the CryptoPack option for EM cores uses ARC Processor EXtension (APEX) technology to accelerate common cryptographic software algorithms.

**ARC SEM Security Processors**

The ARC SEM Family includes the ARCv2 ISA-based ARC SEM110 and SEM120D security processors to protect against logical, hardware and physical attacks. The SEM processors include SecureShield™ technology with a secure MPU that enables the creation of a Trusted Execution Environment (TEE) to protect secure functions from software vulnerabilities that may exist in user code. The ARC SEM110 is a 32-bit RISC core that is optimized for performance, power, and area efficiency. The ARC SEM120D has an added DSP instruction set and unified multiply/ MAC unit. The ARC CryptoPack, FPU and µDMA licensable options are available for the ARC SEM processors.

**ARC HS Processors**

The ARC HS Family, based on the efficient ARCv2 instruction set architecture (ISA), includes the HS34, HS36, HS38, HS44, HS46, HS48, HS45D and HS47D processors. All HS processors support...
closely coupled memories (CCMs), which enable single-cycle access to instructions and data. The HS36, HS38, HS46, HS47D and HS48 add up to 64 KB each of instruction and data caches. The HS38 and HS48 also include an advanced memory management unit (MMU) to support Linux and other high-end operating systems.

The ARC HS4x family features a high-speed 10-stage, dual-issue pipeline that supports out-of-order execution. The HS45D and HS47D support more than 150 DSP-optimized instructions, delivering a unique combination of high-performance control and high-efficiency digital signal processing. The ARC HS4xD processors are compatible with the ultra-low power ARC EMxD processors and have the same instruction set, making it easy to migrate code between the two processor families. HS processors are optimized for GHz+ operating speeds with minimum area and power consumption, making them ideally suited for embedded applications with very high-performance requirements. The HS processors are available in single-core, dual-core and quad-core configurations.

**ARCv1 ISA-Based Processor Families**

The ARC 600, ARC 700 and AS2xx processor families are based on the ARCv1 ISA. The ARC 600 and ARC 700 product lines are general purpose processor cores extensively deployed in high-volume production. Target applications range from deeply embedded control to DSP-intensive processing and Linux host. The ARC AS200 Family includes the AS211SFX and AS221BD audio processors. These processors feature powerful audio processing capabilities and support a broad portfolio of certified audio codecs and post-processing software from a range of popular standards including Dolby®, DTS® and Microsoft®.

**ARC Processor EXtension (APEX) Technology**

ARC processors support the addition of user-defined extensions to the core. These extensions can take the form of more processor and auxiliary registers, new instructions, and/or additional condition code tests. Custom instructions enable designers to efficiently add their proprietary hardware to the processor to further increase application performance.

**ARC VPX DSP Processor**

The ARC VPX5 Processor is based on an extended ARCv2DSP instruction set architecture and optimized for a broad range of high-performance signal processing applications such as RADAR/LiDAR, sensor fusion, and baseband communications processing. The VPX5 DSP processor implements a configurable, energy-efficient very long instruction word (VLIW)/single instruction-multiple data (SIMD) architecture that combines scalar and vector execution units to enable a high degree of parallel processing. The ARC VPX5 DSP processor is supported by the ARC MetaWare Development Toolkit, which provides a comprehensive software programming environment including optimizing vector compiler, debugger, instruction set simulator, and libraries with DSP and math functions.

**Embedded Vision Processors**

The ARC EV7x Embedded Vision processors are fully programmable and configurable IP cores that have been optimized for artificial intelligence and deep learning applications, combining the flexibility of software solutions with the low cost and low power consumption of hardware. The EV7x Processors integrate scalar, vector DSP and deep neural network (DNN) processing units for highly accurate and fast vision processing. The ARC EV7x Vision Processors integrate up to four enhanced vector processing units (VPUs) and a DNN accelerator with up to 14,080 MACs to deliver up to 35 TOPS performance in 16-nanometer (nm) FinFET process technologies under worst case conditions, 4X the performance of the ARC EV6x processors.

The EV Processors are designed to integrate seamlessly into an SoC and can be used with any host processors and operate in parallel with the host. With up to four vector DSPs that operate in parallel to the DNN engine, the EV7x Processors provide scalable performance that supports convolutional neural network (CNN) and recurrent neural network (RNN) graphs. In addition, an optional IEEE 754-compliant vector floating point unit, integrated into the vector DSP core, and its supporting software, offer performance levels of up to 328 Gigaflops for single precision operations and 655 Gigaflops for half precision operations. The embedded deep neural network engine accelerates the processing of CNN/RNN executables, enabling accurate and power-efficient object detection, image classification, and convolutional LSTMs.

The DesignWare ARC Functional Safety Processors offer optional AES-XTS encryption engines to protect data passing from on-chip memory to the vision engine and DNN accelerator. The AES-XTS engine prevents high-value data such as training datasets and personal biometric data, including facial recognition and retina scans, from being exploited.

**ARC Functional Safety Processors**

The DesignWare ARC functional safety (FS) processors support ASIL B and ASIL D safety levels to simplify safety-critical automotive SoC development and accelerate ISO 26262 qualification. The portfolio includes the ARC EM22FS, HS4xFS, VPX5FS, and EV7xFS safety processors with integrated hardware safety features such as redundant processors, error-correcting code (ECC), parity...
Audio Post-processing S/W
Multi-core Media Framework, MM MQX
(DSP library, peripheral I/O drivers (bare metal),
reference designs ARC Sensor & Control
peripheral I/O drivers (bare metal),
DSP library, audio processing library,
peripheral I/O drivers (bare metal),
reference designs ARC Sensor & Control
peripheral I/O drivers (bare metal),
DSP library, peripheral I/O drivers
(bare metal)

Table 1: DesignWare ARC Processor Subsystems
Simulators

Synopsys offers a variety of simulation products spanning automatically-generated, cycle-accurate simulators to fast, functional instruction-set simulators (ISS). Synopsys’ simulation products enable software development prior to silicon being available.

The DesignWare ARC nSIM Pro Simulator is primarily used for software development and debugging. It can operate as a very fast ISS and also supports the Synopsys Virtualizer prototyping tools. It includes a Virtualizer Development Kit (VDK) for an ARC HS38-based system. This system can boot Linux on the ARC HS38 and can be used for early software development.

DesignWare ARC xCAM is a 100% cycle-accurate simulator that is primarily used for hardware verification, but can also be used to do final optimizations of critical software routines. The xCAM model is automatically generated from the processor configuration and can be used to evaluate different hardware scenarios.

Operating Systems

To support applications that require fast, real-time response, Synopsys offers MQX RTOS. MQX occupies a very small memory footprint and supports fast context switch times.

ARC processor cores with MMUs are supported by a Linux kernel available from the official Linux archive. Synopsys maintains and optimizes the Linux kernel to run optimally on ARC processor cores.

embARC.org

The embARC.org website provides online access to a wide range of open source software and documentation for ARC processors. It provides access to downloads, documentation, mailing lists for open source projects such as ARC Linux and the embARC Open Software Platform. It also includes links to development tools and other resources for developing software on ARC processor-based systems. Users can contribute to this open source software and provide suggestions on improving or adding to the existing open source projects.

Available on embARC.org, the embARC Open Software Platform is an easily accessible, highly productive solution for developing software for ARC EM and HS processor-based embedded systems and subsystems, especially those targeting the IoT. The comprehensive suite of free and open-source software available from the embARC.org website, including drivers, operating systems and middleware, enables code development to start sooner and complete faster. Documentation and other resources available on the website facilitate the sharing of information and expertise among the ARC-based development community.

Third-party Ecosystem

The ARC Access Program expands the choice of embedded software and hardware solutions available for ARC processor cores. This program builds on the ecosystem of third parties supporting the ARC architecture with software development tools, real-time operating systems (RTOSes), middleware and semiconductor IP.

The ARC Access Program helps customers to:

• Develop ARC-based embedded solutions faster by leveraging compatible products from leading embedded industry vendors
• Reduce project risk by taking advantage of design solutions pre-ported and tested for the DesignWare ARC architecture
• Save on development costs and resources by using products optimized for ARC-based designs

ARC EM Software Development Platform

The ARC EM Software Development Platform accelerates software development and debug of ARC EM processor-based system-on-chips (SoCs) for a wide range of ultra-low power embedded applications such as IoT, sensor fusion, and voice applications. The ARC EM Software Development Platform includes a configurable hardware board with commonly used peripherals including motion sensors, flash memory, Bluetooth, and Wi-Fi and is extensible with Arduino, mikroBUS and Pmod connectors. Downloadable platform packages with hardware and software configuration information are available, providing a flexible software development platform.

ARC IoT Development Kit

The DesignWare ARC IoT Development Kit accelerates software development and debug of ARC EM processor-based SoC designs.
The kit includes a silicon implementation of the ARC Data Fusion IP Subsystem as well as a rich set of peripherals commonly used in IoT designs such as USB, I3C and PWM. The kit is supported by Synopsys’ MetaWare Development ToolKit, which includes a compiler, debugger and libraries optimized for maximum performance with minimal code size.

**ARC EM Starter Kit**

The ARC EM Starter Kit is a low-cost, versatile solution enabling rapid software development, code porting, software debugging, and system analysis for ARC EM processors. The kit consists of a small factor board with pre-installed FPGA images supporting the range of EM cores including the EM4, EM5D, EM6 and EM7D, as well as FPU. Software support includes MQX RTOS and the embARC Open Software platform available from the [embARC.org](http://embARC.org) web portal.

**ARC HS Development Kit**

The ARC HS Development Kit is a ready-to-use software development platform that includes a multicore ARC HS-based chip, implemented in a TSMC 28HPM process, that integrates a wide range of interfaces including Ethernet, USB, SDIO, I2C, SPI, UART, and GPIO, as well as a Vivante GC7000 Nano Ultra GPU. The kit also features an on-board WiFi and Bluetooth module. This combination of ARC HS processors and the comprehensive set of peripherals allow developers to build and debug complex software on a fully-featured hardware platform. Software support includes ARC Linux and the embARC Open Software platform available from the [embARC.org](http://embARC.org) web portal.

**ARC AXS10x Software Development Platforms**

The DesignWare ARC Software Development Platforms are complete, standalone platforms enabling software development, code porting, software debugging and system analysis. They consist of an ARC CPU card mounted on an ARC Software Development Platform mainboard. The CPU cards have an associated software package of pre-built operating systems, drivers and examples. Readily licensable DesignWare IP has been used to build the ARC Software Development Platforms, giving the systems a rich set of peripherals that can also be implemented in an SoC. The ARC Software Development Platforms can easily be combined with the Synopsys HAPS® FPGA-Based Prototyping Solution to enable system prototyping and additional extension interfaces, such as five Digilent Pmod™ Compatible connectors, support the integration of other custom and commercially available hardware extensions.

**ASIP Designer**

Modern multicore SoCs often include specialized processing functions that sometimes cannot be addressed efficiently with off-the-shelf processor IP. These custom processing elements are often manually designed, requiring significant engineering effort and lacking ease-of-use features such as programmability. Application-specific instruction-set processors (ASIPs) close this gap.

ASIPs are software-programmable hardware (e.g., custom processors or programmable accelerators) tailored to a specific application or class of algorithms. They are ideally suited for specialized DSP applications, enabling designers to take advantage of inherent instruction- and data-level parallelism and customized datapath elements to achieve high levels of performance in a minimal power envelope. Because they are programmable, ASIPs
also give design teams the flexibility to support post-silicon modifications as well as specifications that are still evolving.

ASIP Designer is a tool suite to accelerate the design and verification of ASIPs that brings ASIP design within easy reach of every SoC team. Using a single processor description language, ASIP Designer automatically generates both a software development kit (SDK) including a C/C++ compiler, both cycle-accurate and instruction-accurate simulators, and a fully featured debugger, as well as synthesizable RTL. This allows for efficient exploration of architectural choices and a rapid path to silicon implementation.

### DesignWare Processor Families

| ARC EM Family—Ultra-Compact, Ultra Low-Power Processors for Deeply Embedded Applications |
|----------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| **Key Features**                       | EM4    | EM6    | EM5D   | EM7D   | EM9D   | EM11D  | EM22FS |
| 3-stage pipeline based on AR Cv2 ISA   | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| Up to 2 MB instruction and data closely coupled memory | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| Enhanced sleep modes                  | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| Arm® AMBA® AHB and AHB-Lite™ interfaces | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| 32 KB of instruction and data caches  | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| DSP enhanced AR Cv2DSP ISA with 150+ DSP instructions and 32x32 MUL/MAC | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| Up to 8 registers for fast context switch | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| Programmable watchdog timer           | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| 32x32 MUL/MAC unit                    | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| XY memory                             |        | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| Power management interface/DVFS support | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| ECC on memories                       | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      | ✔      |
| Enhanced Security Package             | Opt    | Opt    |        | ✔      | ✔      | ✔      | ✔      |
| Memory Protection Unit (MPU)          | Opt    | Opt    | Opt    | Opt    | Opt    | Opt    | ✔      |
| **Example Applications**              | IoT, wearables, sensor processing and control, smart appliances, always-on sensors, SSDs, flash controllers, automotive safety systems (ISO 26262)  |

Opt = separately licensable options
DesignWare Processor Families (Continued)

### ARC SEM Family—Security Processors for Low-Power Embedded Applications

<table>
<thead>
<tr>
<th>Key Features</th>
<th>SEM110</th>
<th>SEM120D</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-stage pipeline based on ARCV2 ISA</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Up to 2 MB instruction and data closely coupled memory</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Secure privilege mode orthogonal to kernel/user mode</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Enhanced secure MPU with context ID for secure or normal operation</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Up to 16 configurable protected regions and per region scrambling capability</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Uniform instruction timing</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Timing/power randomization</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>In-line instruction scrambling</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Data and instruction path integrity checking</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Integrated watchdog timer</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Secure debug capability with user-defined challenge/response mechanism</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>DSP-enhanced ARCV2DSP ISA with 100+ DSP instructions and 32x32 MUL/MAC</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>µDMA controller</td>
<td>Opt</td>
<td>Opt</td>
</tr>
<tr>
<td>CryptoPack (cryptographic software algorithm acceleration)</td>
<td>Opt</td>
<td>Opt</td>
</tr>
<tr>
<td>FPU (single- and double-precision, IEEE754-2008 compliant)</td>
<td>Opt</td>
<td>Opt</td>
</tr>
</tbody>
</table>

#### Example Applications

IoT industrial, smart cities, smart meters, embedded SIM, healthcare

*Opt = separately licensable options*

### ARC HS Family—High-Speed 32-bit Processors for High-End Embedded Applications

<table>
<thead>
<tr>
<th>Key Features</th>
<th>HS34</th>
<th>HS36</th>
<th>HS38</th>
<th>HS44</th>
<th>HS46</th>
<th>HS48</th>
<th>HS45D</th>
<th>HS47D</th>
<th>HS46FS</th>
<th>HS47DFS</th>
<th>HS48FS</th>
</tr>
</thead>
<tbody>
<tr>
<td>10-stage pipeline based on ARCV2 ISA</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Dual-issue pipeline</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Up to 16 MB instruction and data closely coupled memory (CCM)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>64-bit loads and stores</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Up to 8 register files for fast context switching</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Arm® AMBA® AXI™ and AHB-Lite™ interfaces</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Single-, dual- and quad-core configurations</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>64 KB of instruction and data caches</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Enhanced sleep modes and architectural clock gating</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>DSP enhanced ARCV2DSP with 150+ DSP instructions</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>L1 and I/O cache coherency</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>64-bit ARC Processor EXtensions (APEX)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>ECC on memories</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>32x32 MUL/MAC unit</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
## DesignWare Processor Families (Continued)

### ARC HS Family—High-Speed 32-bit Processors for High-End Embedded Applications

<table>
<thead>
<tr>
<th>Feature</th>
<th>VPX5</th>
<th>VPX5FS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power management interface/DVFS support</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Memory Management Unit (MMU) supporting 40-bit addressing</td>
<td>Opt</td>
<td>✓</td>
</tr>
<tr>
<td>L2 cache</td>
<td>Opt</td>
<td>✓</td>
</tr>
<tr>
<td>Enhanced Security Package</td>
<td>Opt</td>
<td>✓</td>
</tr>
<tr>
<td>FPU (single- and double-precision, IEEE754-2008 compliant)</td>
<td>Opt</td>
<td>✓</td>
</tr>
<tr>
<td>Memory Protection Unit (MPU)</td>
<td>Opt</td>
<td>✓</td>
</tr>
<tr>
<td>Cluster DMA</td>
<td>Opt</td>
<td>✓</td>
</tr>
<tr>
<td>Real-Time Trace (RTT)</td>
<td>Opt</td>
<td>✓</td>
</tr>
</tbody>
</table>

**Example Applications**
- Solid state drive (SSD) controller, automotive systems, home gateways, baseband control, home networking, edge devices, embedded Linux-based devices

*Opt = separately licensable options*

### ARC VPX Family—High-Performance DSP for Signal Processing Applications

<table>
<thead>
<tr>
<th>Key Features</th>
<th>VPX5</th>
<th>VPX5FS</th>
</tr>
</thead>
<tbody>
<tr>
<td>AR Cv2 ISA support</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Scalar execution unit</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Three vector execution units</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Dual SIMD multiply units (8-, 16- and 32-bit)</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Dual floating point vector engines (half and single precision)</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Linear algebra/math vector floating point engine</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Vector data closely coupled memory (VCCM)</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Arm® AMBA® AXI™ and AHB-Lite™ interfaces</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Single-, dual- and quad-core configurations</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Enhanced sleep modes and architectural clock gating</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>L1 and I/O cache coherency unit</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>ECC on memories</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Safety certified</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Power management interface/DVFS support</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>L2 cache</td>
<td>Opt</td>
<td>Opt</td>
</tr>
<tr>
<td>Scalar FPU (single- and double-precision, IEEE754-2008 compliant)</td>
<td>Opt</td>
<td>Opt</td>
</tr>
<tr>
<td>Memory Protection Unit (MPU)</td>
<td>Opt</td>
<td>Opt</td>
</tr>
<tr>
<td>2D DMA engine</td>
<td>Opt</td>
<td>Opt</td>
</tr>
<tr>
<td>Real-Time Trace (RTT)</td>
<td>Opt</td>
<td>Opt</td>
</tr>
</tbody>
</table>

**Example Applications**
- Automotive driver assist systems (ADAS), RADAR, LiDAR, powertrain, sensor fusion, baseband communications, industrial automation, smart home, IoT

*Opt = separately licensable options*
### DesignWare Processor Families (Continued)

#### EV Family—Fast, Accurate Object Detection for Embedded Vision Applications

<table>
<thead>
<tr>
<th>Key Features</th>
<th>EV71</th>
<th>EV72</th>
<th>EV74</th>
<th>EV71FS</th>
<th>EV72FS</th>
<th>EV74FS</th>
<th>EV61</th>
<th>EV62</th>
<th>EV64</th>
</tr>
</thead>
<tbody>
<tr>
<td># vector processing units</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Vision engine MACs</td>
<td>54</td>
<td>128</td>
<td>256</td>
<td>54</td>
<td>128</td>
<td>256</td>
<td>54</td>
<td>128</td>
<td>256</td>
</tr>
<tr>
<td>DMA option</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>L1 cache coherency</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>DNN/CNN Engine option (MACs)</td>
<td>880, 1760, 3520, 7K or 14K</td>
<td>880, 1760, 3520, 7K or 14K</td>
<td>880, 1760, 3520, 7K or 14K</td>
<td>880, 1760, 3520, 7K or 14K</td>
<td>880, 1760, 3520, 7K or 14K</td>
<td>880, 1760, 3520, 7K or 14K</td>
<td>880, 1760, 3520</td>
<td>880, 1760, 3520</td>
<td>880, 1760, 3520</td>
</tr>
<tr>
<td>Vector floating point unit option</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Real-time trace (RTT)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Safety certified</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>AES Encryption option</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

**Example applications**

Autonomous vehicles, ADAS, surveillance, facial detection/recognition, augmented reality, SLAM

#### ARC AS200 Audio Family—Efficient Single/Dual Core Audio Processors, Optimized Codecs

<table>
<thead>
<tr>
<th>Key Features</th>
<th>AS211SFX</th>
<th>AS221BD</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-stage pipeline</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Dual MAC with 80-bit accumulator</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>AMBA AXI or BVICI interfaces</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>ARC-optimized audio codecs support Dolby, DTS, Microsoft, SRS technologies and more</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Dual-core configuration</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Floating point extensions (single and double-precision, IEEE compliant)</td>
<td>Opt</td>
<td>Opt</td>
</tr>
<tr>
<td>Memory Protection Unit (MPU)</td>
<td>Opt</td>
<td>Opt</td>
</tr>
<tr>
<td>Real-Time Trace (RTT)</td>
<td>Opt</td>
<td>Opt</td>
</tr>
</tbody>
</table>

**Example Applications**

Portable audio players, digital TVs, set-top boxes, sound bars, multi-channel HD, wireless headsets and speakers

Opt = separately licensable options

### About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys’ IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys’ extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

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