

DesignWare Processor IP Portfolio

- Scalable family of 32-bit processor cores, vision processors, and subsystems
- Maximum power and area efficiency (DMIPS/mW, DMIPS/mm²) for embedded applications
- Highly configurable so each instance can be optimized
- Extensible instruction set enables application-specific customizations
- Integrated tool suite with broad hardware and software ecosystem support



DesignWare Processor IP Portfolio

| ARC HS Family High-performance control | ARC EM Family Ultra-low power embedded processing | ARC SEM Family Security processors for embedded applications | EV Family Embedded vision |
|--|---|--|--|
| <ul style="list-style-type: none"> · Highest performance ARC cores · Single or dual issue · High-speed 10-stage pipeline, SMP Linux support · Single-, dual-, quad-core configurations | <ul style="list-style-type: none"> · Optimized for ultra-low power · 3-stage pipeline RISC processors with RISC + DSP · Maximum performance and area-efficiency: up to 1.77 DMIPS/MHz and as small as 0.01mm² | <ul style="list-style-type: none"> · Power- and area-efficient security processors for IoT and mobile applications · Protection against hardware, software and side channel attacks · SecureShield for Trusted Execution Environments | <ul style="list-style-type: none"> · Multicore design optimized for vision processing · Wide vector DSP and programmable convolution neural network engine · 5X better power efficiency than existing solutions · ASIL B, C or D Ready options for safety-critical designs |

Processor IP

Synopsys' processor IP portfolio includes the DesignWare® ARC® and EV Processor families as well as IP subsystems, software, development systems and tools. ARC processor cores are based on a flexible and proven 32-bit instruction set architecture (ISA) with features optimized for a broad range of embedded and deeply embedded applications:

- Performance-efficient designs deliver maximum performance while consuming a minimum amount of power and silicon area
- Highly configurable processors can be performance- and power-optimized for each instance on an SoC while sharing a common programming model
- Extensible ISA supports user-defined custom instructions, enabling integration of users' proprietary hardware to accelerate application-specific tasks
- Streamlined system integration through the ability to closely couple memory and directly map peripherals to the core, reducing system latency and cost

ARC HS Processors

The ARC HS Family, based on the efficient ARCv2 instruction set architecture (ISA), includes the HS34, HS36, HS38, HS44, HS46, HS48, HS45D and HS47D processors. All HS processors support closely coupled memories (CCMs), which enable single-cycles access to instructions and data. The HS36 adds up to 64 KB each of instruction and data caches, and the HS38 includes an advanced memory management unit (MMU) to support Linux and other high-end operating systems.

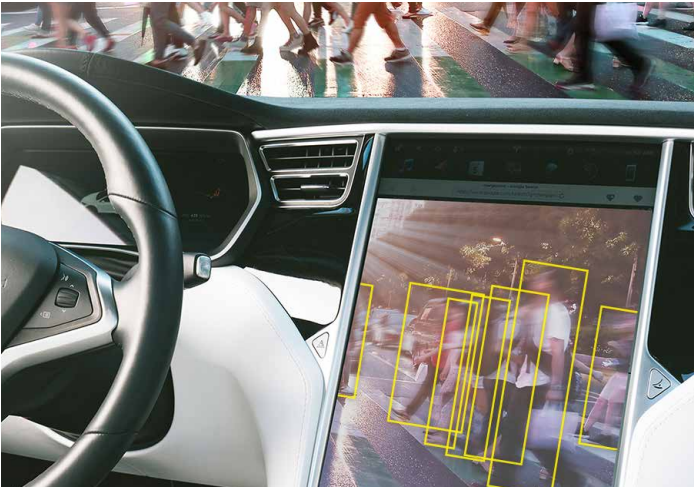
The ARC HS4x family features a high-speed 10-stage, dual-issue pipeline that supports out-of-order execution. The HS45D and HS47D support more than 150 DSP-optimized instructions, delivering a unique combination of high-performance control and high-efficiency digital signal processing. The ARC HS4xD processors are compatible with the ultra-low power ARC EMxD processors and have the same instruction set, making it easy to

migrate code between the two processor families. HS processors are optimized for GHz+ operating speeds with minimum area and power consumption, making them ideally suited for embedded applications with very high-performance requirements. The HS processors are available in single-core, dual-core and quad-core configurations.

ARC EM Processors

The ARC EM Family includes the ARCv2 ISA-based ARC EM4 and EM6 as well as the DSP-enhanced EM5D, EM7D, EM9D and EM11D. The ARC EM4, EM5D and EM9D processors support instruction and data CCMs and the EM6, EM7D and EM11D additionally support instruction and data caches. The EM9D and EM11D feature support for XY memories to deliver higher levels of signal processing efficiency. The EM family also includes the ASIL D-Ready EM4SI and EM5DSI Safety Islands, pre-verified dual lockstep implementations including a self-checking safety monitor for safety-critical automotive applications. The ultra-compact EM cores feature excellent code density, small size and very low power consumption, making them ideal for power-critical and area-sensitive embedded and deeply embedded applications.





Along with optional FPU, MPU, μ DMA, Real-Time Trace and ARConnect for multicore integration, the EM Family also offers a Safety Enhancement Package option, which includes safety documentation, integrated hardware safety features and a certified ASIL-D ready compiler to help automotive designers achieve ISO 26262 safety compliance.

To address system security, an optional Enhanced Security Package provides tamper protection features and enables designers to create a trusted execution environment that protects their systems and software from evolving security threats such as IP theft and intentional remote attacks. In addition, the CryptoPack option for EM cores uses ARC Processor EXTension (APEX) technology to accelerate common cryptographic software algorithms.

ARC SEM Security Processors

The ARC SEM Family includes the ARCV2 ISA-based ARC SEM110 and SEM120D security processors to protect against logical, hardware and physical attacks. The SEM processors include SecureShield™ technology with a secure MPU that enables the creation of a Trusted Execution Environment (TEE) to protect secure functions from software vulnerabilities that may exist in user code. The ARC SEM110 is a 32-bit RISC core that is optimized for performance, power, and area efficiency. The ARC SEM120D has an added DSP instruction set and unified multiply/ MAC unit. The ARC CryptoPack, FPU and μ DMA licensable options are available for the ARC SEM processors.

ARCV1 ISA-Based Processor Families

The ARC 600, ARC 700 and AS2xx processor families are based on the ARCV1 ISA. The ARC 600 and ARC 700 product lines are general purpose processor cores extensively deployed in high-volume production. Target applications range from deeply embedded control to DSP-intensive processing and Linux host. The ARC AS200 Family includes the AS211SFX and AS221BD audio processors. These processors feature powerful audio processing capabilities and support a broad portfolio of certified audio codecs and post-processing software from a range of popular standards including Dolby®, DTS® and Microsoft®.

ARC Processor EXTension (APEX) Technology

ARC processors support the addition of user-defined extensions to the core. These extensions can take the form of more processor and auxiliary registers, new instructions, and/or additional condition code tests. Custom instructions enable designers to efficiently add their proprietary hardware to the processor to further increase application performance.

Embedded Vision Processors

The DesignWare EV6x Embedded Vision processors are fully programmable and configurable IP cores that have been optimized for artificial intelligence and deep learning applications, combining the flexibility of software solutions with the low cost and low power consumption of hardware. The EV6x Processors integrate scalar, vector DSP and convolutional neural network (CNN) processing units for highly accurate and fast vision processing.

The EV Processors are designed to integrate seamlessly into an SoC and can be used with any host processors and operate in parallel with the host. With up to four vector DSPs that operate in parallel to the CNN engine, the EV6x Processors provide scalable performance that supports all vision algorithms and CNN graphs. In addition, an optional IEEE 754-compliant vector floating point unit, integrated into the vector DSP core, and its supporting software, offer performance levels of up to 328 Gigaflops for single precision operations and 655 Gigaflops for half precision operations. The embedded deep neural network engine accelerates the processing of CNN executables, enabling accurate and power-efficient object detection, image classification and semantic segmentation.

DesignWare EV6x Embedded Vision Processors with Safety Enhancement Package (SEP) provide ASIL B, C, and D Ready processor IP to accelerate the development of automotive system-on-chips (SoCs). The EV6x Processors with SEP option include state-of-the-art safety mechanisms and hardware safety features such as lockstep capabilities, ECC memories, error checking on core registers and safety-critical registers, a dedicated safety monitor, and a windowed watchdog timer for each core. The IP comes with comprehensive safety documentation, including FMEDA reports and safety manuals to accelerate SoC-level functional safety assessments.

To speed application software development, the EV Processors are supported by a comprehensive software programming environment based on embedded vision and neural network standards including OpenCV, OpenCL™ C, OpenVX™ with the DesignWare ARC MetaWare EV Development Toolkit. The toolkit includes a CNN mapping tool that analyzes neural networks trained using popular frameworks like Caffe, and automatically generates the executable for the programmable CNN engine. For maximum flexibility and future-proofing, the tool can also distribute computations between the vision CPU and CNN resources to support new and emerging neural networks. An ASIL D Ready ARC MetaWare EV Development Toolkit for Safety provides a complete set of tools and runtime libraries to speed software development for AI applications requiring EV6x Processors with SEP option.

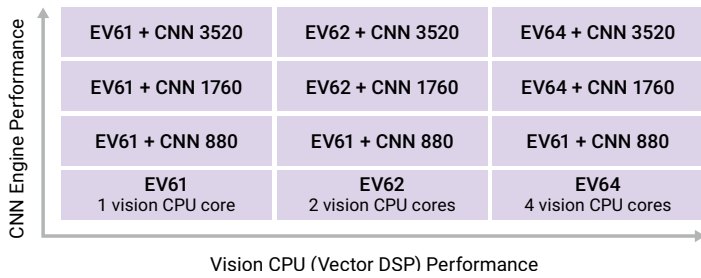


Figure 1: DesignWare EV6x Embedded Vision Processor configuration options

ARC Processor Subsystems

ARC Secure IP Subsystem

The DesignWare ARC Secure IP Subsystem addresses security threats in high-value embedded applications such as integrated SIMs (iSIMs), smart metering and embedded Universal Integrated Circuit Cards (eUICC). The DesignWare ARC Secure IP Subsystem offers the choice of ultra-low power ARC SEM110 and SEM120D Processors with SecureShield technology, which enables secure code execution, secure handling of assets and tamper protection. The Secure IP Subsystem includes both software- and hardware-accelerated cryptography options as well as secure instruction and data memory controllers that provide confidentiality and authenticity for non-trusted memory accesses. The subsystem’s hardware security features are complemented by software, including a NIST-validated cryptography library, SecureShield Runtime Library and secure boot support.

ARC Sensor and Control IP Subsystem

The DesignWare ARC Sensor & Control IP Subsystem is optimized to process data from digital and analog sensors, offloading the host processor and enabling more power-efficient processing of sensor and control data. The fully configurable IP subsystem includes the choice of an ARC EM4 or EM6 processor, serial digital interfaces, data converter interfaces and hardware accelerators. The Sensor

& Control IP Subsystem provides designers with a complete and pre-verified solution that meets the requirements of a broad range of sensor processing and control functions increasingly prevalent in automotive, mobile, industrial and IoT markets.

ARC Data Fusion IP Subsystem

The DesignWare ARC Data Fusion IP Subsystem is a complete, pre-verified, hardware and software solution optimized for a wide range of ultra-low power IoT applications. It is designed for fast and easy integration within a larger system context. The fully configurable ARC Data Fusion IP Subsystem includes the choice of a low gate count and energy-efficient DesignWare ARC EM5D, EM7D, EM9D or EM11D processor for both RISC and DSP processing, accompanied by an extensive collection of I/O functions and fast math (trigonometric) accelerators. The software libraries of the subsystem contain small-footprint drivers for all I/O, plus DSP functions supporting signal processing. It also includes an audio processing software library of common functions, including gain control, mixer and sample rate converter. The integrated solution is optimized for “always on” data fusion combining sensor, voice, gesture and audio processing typically implemented in IoT edge devices.

ARC SoundWave Audio IP Subsystem

The DesignWare ARC SoundWave Audio IP Subsystem provides designers with a complete, pre-verified audio subsystem consisting of hardware, software and prototyping for integration into SoC designs. It consists of DesignWare 32-bit ARC audio processors, standard digital interfaces, analog audio codecs, and a complete, ready-to-use software environment that seamlessly plugs into the host application and includes a comprehensive library of software audio codecs that support the latest formats from Dolby, DTS and SRS. Supporting 2.1 to 7.1 audio streams at 24-bit precision, the SoundWave Audio IP Subsystem meets the demanding performance requirements of today’s audio applications such as digital TVs, set-top boxes, Blu-ray Disc, speaker bars, media players, portable audio and tablets.

| ARC Subsystems | Supported Processors | Hardware Accelerators | Integrated Peripherals | Included Software |
|-------------------------------------|-------------------------|-----------------------|--|--|
| ARC Secure IP Subsystem | SEM110, SEM120D | ✓ | UART, TRNG I/F, Device ID, NVM I/F, GPIO | Crypto library, DSP library (SEM120D), device drivers, secure boot, SecureShield runtime |
| ARC Data Fusion IP Subsystem | EM5D, EM7D, EM9D, EM11D | ✓ | SPI, I2C, I3C, PWM, UART, PDM, ADC I/F, DAC I/F, APB I/F, GPIO | DSP library, audio processing library, peripheral I/O drivers (bare metal), reference designs ARC Sensor & Control |
| ARC Sensor and Control IP Subsystem | EM4, EM6 | ✓ | SPI, I2C, PWM, UART, ADC I/F, DAC I/F, APB I/F, GPIO | DSP library, peripheral I/O drivers (bare metal) |
| ARC SoundWave Audio IP Subsystem | AS211SFX, AS221BD | ✓ | I2S, S/PDIF, Analog Codec I/F, Reset, Clock Management | Multi-core Media Framework, MM MQX Audio Post-processing S/W |

Table 1: DesignWare ARC Processor Subsystems



DesignWare ARC xCAM is a 100% cycle-accurate simulator that is primarily used for hardware verification, but can also be used to do final optimizations of critical software routines. The xCAM model is automatically generated from the processor configuration and can be used to evaluate different hardware scenarios.

Operating Systems

To support applications that require fast, real-time response, Synopsys offers MQX RTOS. MQX occupies a very small memory footprint and supports fast context switch times.

ARC processor cores with MMUs are supported by a Linux kernel available from the official Linux archive. Synopsys maintains and optimizes the Linux kernel to run optimally on ARC processor cores.

embARC.org

The embARC.org web site provides online access to a wide range of open source software and documentation for ARC processors. It provides access to downloads, documentation, mailing lists for open source projects such as ARC Linux and the embARC Open Software Platform. It also includes links to development tools and other resources for developing software on ARC processor-based systems. Users can contribute to this open source software and provide suggestions on improving or adding to the existing open source projects.

Available on embARC.org, the embARC Open Software Platform is an easily accessible, highly productive solution for developing software for ARC EM and HS processor-based embedded systems and subsystems, especially those targeting the IoT. The comprehensive suite of free and open-source software available from the embARC.org website, including drivers, operating systems and middleware, enables code development to start sooner and complete faster. Documentation and other resources available on the website facilitate the sharing of information and expertise among the ARC-based development community.

Third-party Ecosystem

The ARC Access Program expands the choice of embedded software and hardware solutions available for ARC processor cores. This program builds on the ecosystem of third parties supporting the ARC architecture with software development tools, real-time operating systems (RTOSes), middleware and semiconductor IP.

The ARC Access Program helps customers to:

- Develop ARC-based embedded solutions faster by leveraging compatible products from leading embedded industry vendors
- Reduce project risk by taking advantage of design solutions pre-ported and tested for the DesignWare ARC architecture
- Save on development costs and resources by using products optimized for ARC-based designs

Software Development Support

Software Tool Chains

To accelerate the SoC development cycle, Synopsys' processor IP is supported by a complete and integrated development tool suite, including tools for configuration, software development and simulation. This enables ARC users to efficiently build, debug, profile and optimize their embedded software applications for ARC.

The ARC MetaWare Development Toolkit contains all the components needed to support the development, debugging and optimization of embedded applications for ARC processors. The compiler and debugger are fully integrated in the Eclipse-based MetaWare Integrated Development Environment (IDE), and the Toolkit also comes with a base version of the nSIM Instruction-Set Simulator.

In addition, Synopsys' ARC processors are supported by the latest open-source GNU Tool Chain, including the GNU GCC Compiler, GDB Debugger, libraries and utilities.

Simulators

Synopsys offers a variety of simulation products spanning automatically-generated, cycle-accurate simulators to fast, functional instruction-set simulators (ISS). Synopsys' simulation products enable software development prior to silicon being available.

The DesignWare ARC nSIM Pro Simulator is primarily used for software development and debugging. It can operate as a very fast ISS and also supports the Synopsys Virtualizer prototyping tools. It includes a Virtualizer Development Kit (VDK) for an ARC HS38-based system. This system can boot Linux on the ARC HS38 and can be used for early software development.

ARC IoT Development Kit

The DesignWare ARC IoT Development Kit accelerates software development and debug of ARC EM processor-based SoC designs. The kit includes a silicon implementation of the ARC Data Fusion IP Subsystem as well as a rich set of peripherals commonly used in IoT designs such as USB, I3C and PWM. The kit is supported by Synopsys' MetaWare Development ToolKit, which includes a compiler, debugger and libraries optimized for maximum performance with minimal code size.



Figure 2: ARC IoT Development Kit

ARC HS Development Kit

The ARC HS Development Kit is a ready-to-use software development platform that includes a multicore ARC HS-based chip, implemented in a TSMC 28HPM process, that integrates a wide range of interfaces including Ethernet, USB, SDIO, I2C, SPI, UART, and GPIO, as well as a Vivante GC7000 Nano Ultra GPU. The kit also features an on-board WiFi and Bluetooth module. This combination of ARC HS processors and the comprehensive set of peripherals allow developers to build and debug complex software on a fully-featured hardware platform. Software support includes ARC Linux and the embARC Open Software platform available from the embARC.org web portal.

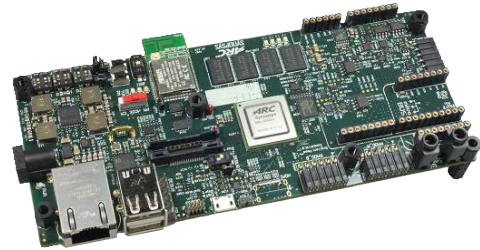


Figure 4: ARC HS Development Kit

ARC EM Starter Kit

The ARC EM Starter Kit is a low-cost, versatile solution enabling rapid software development, code porting, software debugging, and system analysis for ARC EM processors. The kit consists of a small factor board with pre-installed FPGA images supporting the range of EM cores including the EM4, EM5D, EM6 and EM7D, as well as FPU. Software support includes MQX RTOS and the embARC Open Software platform available from the embARC.org web portal.



Figure 3: ARC EM Starter Kit

ARC AXS10x Software Development Platforms

The DesignWare ARC Software Development Platforms are complete, standalone platforms enabling software development, code porting, software debugging and system analysis. They consist of an ARC CPU card mounted on an ARC Software Development Platform mainboard. The CPU cards have an associated software package of pre-built operating systems, drivers and examples. Readily licensable DesignWare IP has been used to build the ARC Software Development Platforms, giving the systems a rich set of peripherals that can also be implemented in an SoC. The ARC Software Development Platforms can easily be combined with the Synopsys HAPS® FPGA-Based Prototyping Solution to enable system prototyping and additional extension interfaces, such as five Digilent Pmod™ Compatible connectors, support the integration of other custom and commercially available hardware extensions.

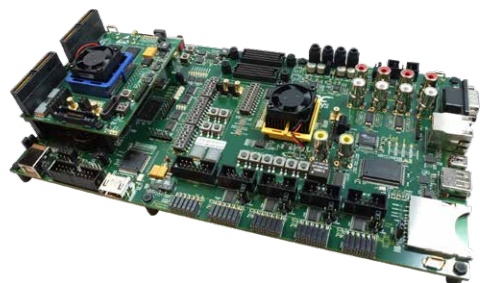


Figure 5: ARC AXS103 Software Development Platform

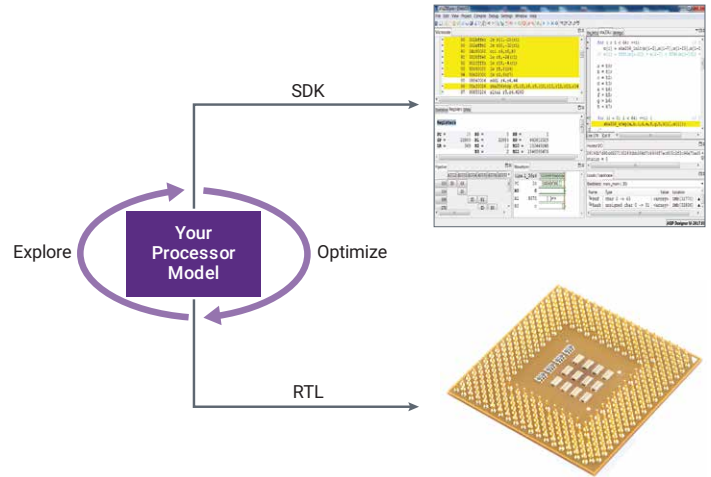
ASIP Designer

Modern multicore SoCs often include specialized processing functions that sometimes cannot be addressed efficiently with off-the-shelf processor IP. These custom processing elements are often manually designed, requiring significant engineering effort and lacking ease-of-use features such as programmability. Application-specific instruction-set processors (ASIPs) close this gap.

ASIPs are software-programmable hardware (e.g., custom processors or programmable accelerators) tailored to a specific application or class of algorithms. They are ideally suited for specialized DSP applications, enabling designers to take advantage of inherent instruction- and data-level parallelism and customized datapath elements to achieve high levels of performance in a minimal power envelope. Because they are programmable, ASIPs also give design teams the flexibility to support post-silicon modifications as well as specifications that are still evolving.

ASIP Designer is a tool suite to accelerate the design and verification of ASIPs that brings ASIP design within easy reach of every SoC team. Using a single processor description language, ASIP Designer automatically generates both a software

development kit (SDK) including a C/C++ compiler, both cycle-accurate and instruction-accurate simulators, and a fully featured debugger, as well as synthesizable RTL. This allows for efficient exploration of architectural choices and a rapid path to silicon implementation.



DesignWare Processor Families

| ARC HS Family—High-Speed 32-bit Processors for High-End Embedded Applications | | | | | | | | |
|---|------|------|------|------|------|------|-------|-------|
| Key Features | HS34 | HS36 | HS38 | HS44 | HS46 | HS48 | HS45D | HS47D |
| 10-stage pipeline based on ARCv2 ISA | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Dual-issue pipeline | | | | ✓ | ✓ | ✓ | ✓ | ✓ |
| Up to 16 MB instruction and data closely coupled memory (CCM) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 64-bit loads and stores | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Up to 8 registers for fast context switching | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Arm® AMBA® AXI™ and AHB-Lite™ interfaces | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Single-, dual- and quad-core configurations | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 64 KB of instruction and data caches | | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| Enhanced sleep modes and architectural clock gating | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| DSP enhanced ARCv2DSP with 150+ DSP instructions | | | | | | | ✓ | ✓ |
| L1 and I/O cache coherency | | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| 64-bit ARC Processor EXTensions (APEX) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ECC on memories | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 32x32 MUL/MAC unit | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Power management interface/DVFS support | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Memory Management Unit (MMU) supporting 40-bit addressing | | Opt | ✓ | | Opt | ✓ | | Opt |
| L2 cache | | Opt | ✓ | | Opt | ✓ | | Opt |
| FPU (single- and double-precision, IEEE754-2008 compliant) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Memory Protection Unit (MPU) | Opt | Opt | | Opt | Opt | | Opt | Opt |
| Real-Time Trace (RTT) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Example Applications | | | | | | | | |
| Solid state drive (SSD) controller, home gateways, digital TV, baseband control, set-top box, home networking, embedded Linux-based devices | | | | | | | | |

Opt = separately licensable options

DesignWare Processor Families (Continued)

| ARC EM Family—Ultra-Compact, Ultra Low-Power Processors for Deeply Embedded Applications | | | | | | | | |
|--|-----|-----|------|------|------|-------|-------|-------|
| Key Features | EM4 | EM6 | EM5D | EM7D | EM9D | EM11D | EM4SI | EM5DS |
| 3-stage pipeline based on ARCV2 ISA | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| Up to 2 MB instruction and data closely coupled memory | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Enhanced sleep modes | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| ARM AMBA AHB, AHB-Lite, and BVCI interfaces | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 32 KB of instruction and data caches | | ✓ | | ✓ | | ✓ | | |
| DSP enhanced ARCV2DSP ISA with 150+ DSP instructions and 32x32 MUL/MAC | | | ✓ | ✓ | ✓ | ✓ | | ✓ |
| Up to 8 registers for fast context switch | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| Programmable watchdog timer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 32x32 MUL/MAC unit | | | ✓ | ✓ | ✓ | ✓ | | ✓ |
| XY memory | | | | | ✓ | ✓ | | |
| Power management interface/DVFS support | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| ECC on memories | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Enhanced Security Package | Opt | | Opt | | | | | |
| Safety Enhancement Package (SEP) for use in ISO 26262 safety-compliant automotive applications | Opt | Opt | Opt | Opt | | | NA | NA |
| μDMA controller | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| CryptoPack (cryptographic software algorithm acceleration) | Opt | Opt | Opt | Opt | Opt | Opt | | |
| FPU (single- and double-precision, IEEE754-2008 compliant) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Memory Protection Unit (MPU) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Real-Time Trace (RTT) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| ARConnect (ARC EM multicore connect IP) | Opt | Opt | Opt | Opt | Opt | Opt | | |
| Example Applications | | | | | | | | |
| IoT, wearables, sensor processing and control, smart appliances, always-on sensors, SSDs, flash controllers, automotive safety systems (ISO 26262) | | | | | | | | |

Opt = separately licensable options

| ARC SEM Family—Security Processors for Low-Power Embedded Applications | | |
|--|--------|---------|
| Key Features | SEM110 | SEM120D |
| 3-stage pipeline based on ARCV2 ISA | ✓ | ✓ |
| Up to 2 MB instruction and data closely coupled memory | ✓ | ✓ |
| Secure privilege mode orthogonal to kernel/user mode | ✓ | ✓ |
| Enhanced secure MPU with context ID for secure or normal operation | ✓ | ✓ |
| Up to 16 configurable protected regions and per region scrambling capability | ✓ | ✓ |
| Uniform instruction timing | ✓ | ✓ |
| Timing/power randomization | ✓ | ✓ |
| In-line instruction scrambling | ✓ | ✓ |
| Data and instruction path integrity checking | ✓ | ✓ |
| Integrated watchdog timer | ✓ | ✓ |
| Secure debug capability with user-defined challenge/response mechanism | ✓ | ✓ |
| DSP-enhanced ARCV2DSP ISA with 100+ DSP instructions and 32x32 MUL/MAC | | ✓ |
| μDMA controller | Opt | Opt |
| CryptoPack (cryptographic software algorithm acceleration) | Opt | Opt |
| FPU (single- and double-precision, IEEE754-2008 compliant) | Opt | Opt |
| Example Applications | | |
| IoT industrial, smart cities, smart meters, embedded SIM, healthcare | | |

Opt = separately licensable options

DesignWare Processor Families (Continued)

| EV Family—Fast, Accurate Object Detection for Embedded Vision Applications | | | |
|--|------|------|------|
| Key Features | EV61 | EV62 | EV64 |
| CNN Engine | Opt | Opt | Opt |
| MACs for vision processing | 944 | 1008 | 1136 |
| DMA for fast, efficient frame data movement | ✓ | ✓ | ✓ |
| Two 32-bit scalar cores | | ✓ | |
| Four 32-bit scalar cores | | | ✓ |
| 512-bit wide vector DSP | ✓ | ✓ | ✓ |
| L1 cache coherency | | ✓ | ✓ |
| Vector Floating Point Unit (FPU); single- and double-precision; IEEE 754 compliant | Opt | Opt | Opt |
| Example Applications | | | |
| Autonomous vehicles, ADAS, surveillance, automotive vision, gesture recognition, face detection/recognition, AR/VR, SLAM | | | |

Opt = separately licensable options

| ARC AS200 Audio Family—Efficient Single/Dual Core Audio Processors, Optimized Codecs | | |
|--|----------|---------|
| Key Features | AS211SFX | AS221BD |
| 5-stage pipeline | ✓ | ✓ |
| Dual MAC with 80-bit accumulator | ✓ | ✓ |
| AMBA AXI or BVCI interfaces | ✓ | ✓ |
| ARC-optimized audio codecs support Dolby, DTS, Microsoft, SRS technologies and more | ✓ | ✓ |
| Dual-core configuration | | ✓ |
| Floating point extensions (single and double-precision, IEEE compliant) | Opt | Opt |
| Memory Protection Unit (MPU) | Opt | Opt |
| Real-Time Trace (RTT) | Opt | Opt |
| Example Applications | | |
| Portable audio players, digital TVs, set-top boxes, sound bars, multi-channel HD, wireless headsets and speakers | | |

Opt = separately licensable options

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes [logic libraries](#), [embedded memories](#), [embedded test](#), [analog IP](#), [wired and wireless interface IP](#), [security IP](#), [embedded processors](#), and [subsystems](#). To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' [IP Accelerated initiative](#) offers [IP prototyping kits](#), IP software development kits, and [IP subsystems](#). Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit [synopsys.com/designware](https://www.synopsys.com/designware).