SYNOPSYS®
Silicon to Software™

DSP Option for ARCv1 Cores

Highlights

- Separate memory banks for X and Y operands
- DMA moves data in and out of XY memory
- Deliver data at register speed
- Eliminate main memory fetch cycles
- High performance address generators
- Address generators operate in several addressing modes
- Fast pointer accesses
- 10% of size of DSP coprocessor
- Single processor solution
- Can replace separate DSP
- Up to 32KB/bank (600 family)
- Up to 64KB/bank (700 family)
- Support for multiple memory banks
- Consolidated development environment for both CPU and DSP

Overview

The DesignWare® ARC® XY option gives designers the ability to add the power of a true DSP engine to ARCv1 CPU cores, enabling conventional and signal processing computation within a single unified architecture. The ARC XY option may be applied to many of the cores within the DesignWare ARC 600 and ARC 700 families.

ARC processor cores that include the XY option provide an optimal solution for many complex computation problems in system-on-chips (SoCs) targeting communications, media processing, storage, security and other embedded applications.

Synopsys also offers DSPlib, a library of frequently used signal processing functions that have been verified and optimized for the ARC XY option. The library takes full advantage of Synopsys' configurable architecture to maximize the performance of each function in the library.

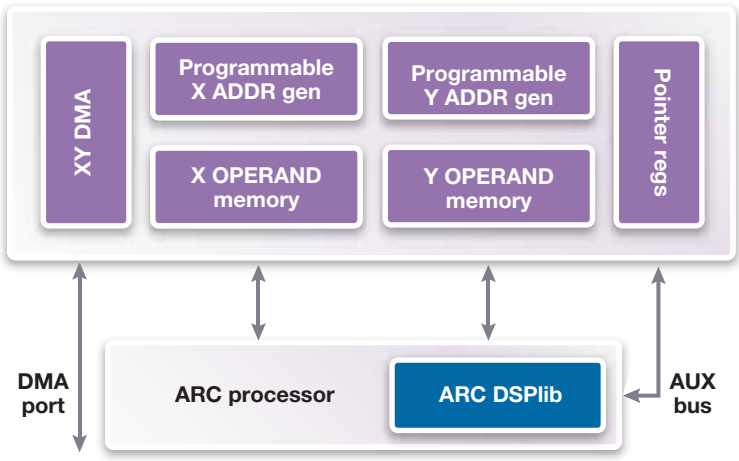

Figure 1. ARC XY option

Applications

- Multimedia codecs
  - Audio/Video decoding andencoding
  - Still image manipulation
- Baseband processing
  - 3G cellular headsets
  - Home gateway
  - Cordless phone
  - COFDM
- Voice
  - Cellular voice codec
  - Voice-over-IP codecs
  - Voice recognition
- Security
  - Encryption acceleration
  - Image recognition
  - Fingerprint identification
  - DRM acceleration

ARC XY Memory Architecture

The ARC XY architecture is built around two memory structures, X and Y, which read two source operands and stores the result in the same cycle. The XY memory is architected to allow instantiation of one or two identical banks. Each bank has its own register set that can be switched when required.

Data in the XY memory is indexed via pointers from address generators and supplied to the ARC CPU pipeline. The memories are software programmable to provide 32-, 16- or dual 16-bit data to the pipeline.

Additionally, an internal DMA engine moves data in and out of XY memory without impacting the processor pipeline.

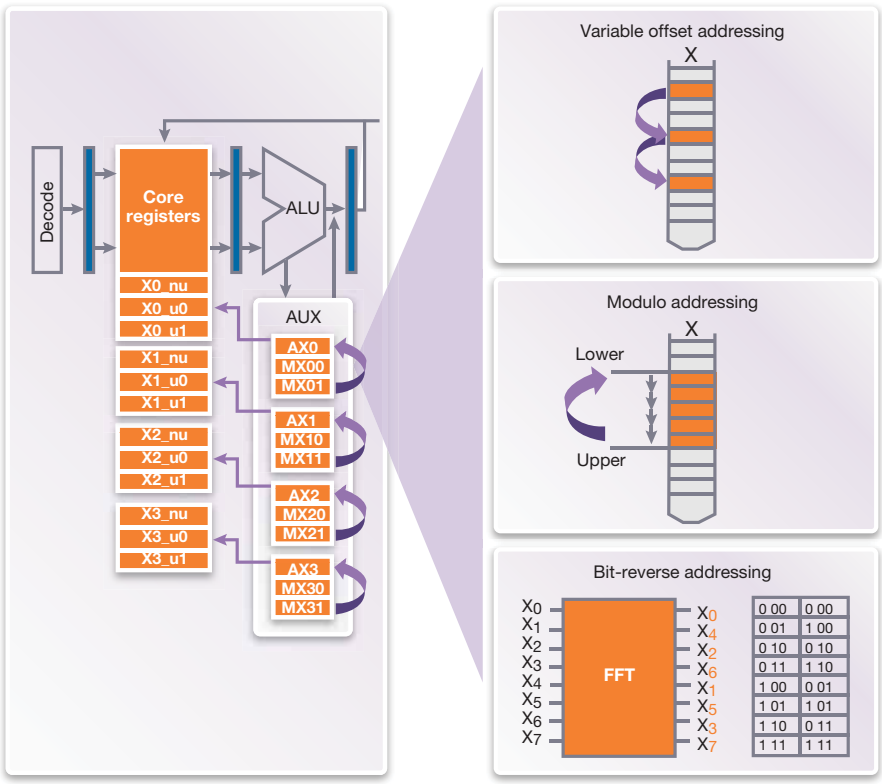

Figure 2. ARC XY memory architecture

DesignWare ARC XY with 600 family core	DesignWare ARC XY with 700 family core
Single or dual port	Dual port
1 or 2 banks	1 bank
1 kb – 32 kb per bank	8 kb – 64 kb

Table 1. Memory configuration options

Address Generator Facilities

The ARC XY option address generators make complex address calculations independently, removing significant overhead from the CPU.

The address generators operate in several addressing modes under software control to optimize performance of DSP algorithms:

- Variable offset
- Modulo
- Bit reverse

The address can be updated after access or remain unchanged based on the instruction.

ARC DSPlib

The ARC DSPlib is a library of instruction extensions developed and verified by Synopsys to accelerate common DSP processing algorithms. By using a the DesignWare ARChitect Processor Configurator tool, designers are able to drag-and-drop instructions from the DesignWare ARC DSPlib and easily apply them to an ARC processor core that has been optimized with the ARC XY option.

Examples of the ARC DSPlib extensions include:

- Dual FFT
- Viterbi
- Cyclic Redundancy Check (CRC)
- 24 x 24 MAC
- SIMD Instructions (Dual Word)

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired interface IP, wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP Prototyping Kits, IP Virtual Development Kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

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