ARC Overlay Management Unit for DesignWare ARC EM Processors

Highlights

- Lightweight hardware-based memory management unit (MMU) enabling address translation and access permission validation
- Fully associative Instruction and Data µTLBs
- Configurable joint TLB depth of 64, 128 or 256 entries
- Common address space for instruction and data
- Independent rd/wr/execute flags for user/kernel modes per page
- Optimized TLB programming with software managed JTLB and hardware assisted replacement policy
- 32-bit unified instruction/data address space
  - 2GB virtual translated address space, mapping to 4GB physical address space
- Configurable page size: 4 KB, 8 KB, 16 KB
- Per page cache control
- Optional ECC for JTLB RAMs

Target Applications

- AIoT
- Storage
- Wireless
- Networking

The DesignWare® ARC® EM Overlay Management Unit (OMU) option enables address translation and access permission validation with minimal power and area overhead while boosting the ability to run larger and more data intensive operations, such as those increasingly prevalent within AIoT, storage and wireless baseband applications, on an ARC EM processor. This hardware-based Overlay Management Unit provides support for virtual memory addressing with a Translation Lookaside Buffer (TLB) for address translation and protection of 4KB, 8KB or 16KB memory pages. In addition, fixed mappings of untranslated memory are supported, enabling the system to achieve increased performance over a large code base residing in a slow secondary storage memory, with the option to be paged in as needed into faster small on-chip page RAM (PRAM) in an efficient way. This is particularly suited for operating environments in which virtual address aliasing is avoided in software.

In systems that run all code as a single process (single PID), using a large virtual address space with a one-to-one correspondence between the virtual address and a large selected area of secondary storage space (such as flash memory or DRAM), the address-translation facility of the Overlay Management Unit can be used to detect when a section (or one or more pages) of code is resident in the PRAM and provide the physical address to the page in the PRAM.

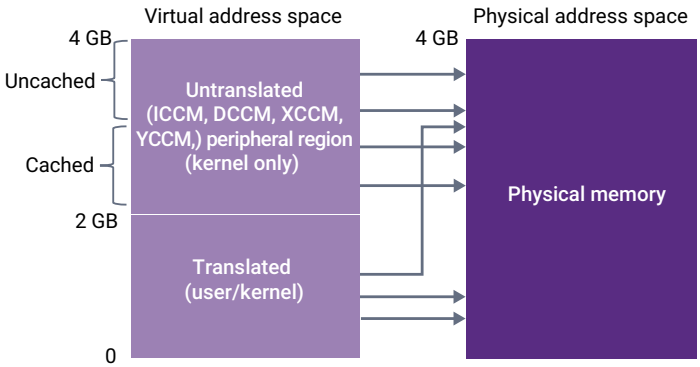

Figure 1: Virtual to Physical Address Translation

Memory Model

The EM processor supports virtual memory addressing when the Overlay Management Unit is present. If the Overlay Management Unit is not present or if it is present but disabled, all the virtual addresses are mapped directly to physical addresses. By default, the Overlay Management Unit is disabled after reset. Note that the data uncached region is always active even if the Overlay Management Unit is disabled.

The Overlay Management Unit features a TLB for address translation and protection of 4 KB, 8 KB or 16 KB memory pages, and fixed mappings of an untranslated memory. The upper half of the untranslated memory section is uncached for I/O uses while the lower half of the untranslated memory is cached for a system kernel.

With the Overlay Management Unit option enabled, the ARC EM cache-based cores define a common address space for both instruction and data accesses in which the memory translation and protection systems can be arranged to provide separate, non-overlapping protected regions of memory for instruction and data access within a common address space. The programming interface to the Overlay Management Unit is independent of the configuration of the TLB in terms of the associativity of number of entries (Figure 2).

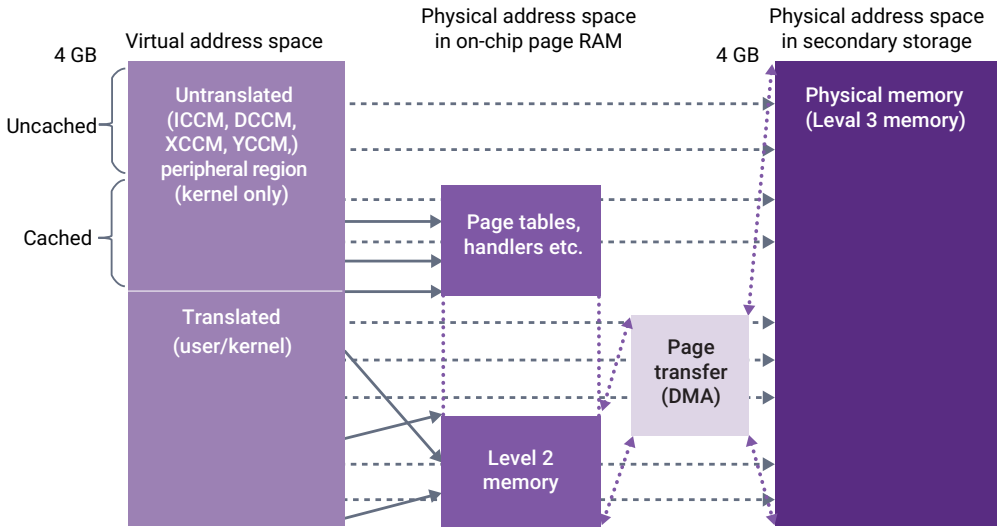

Figure 2: Memory Address Mapping with Overlay Management Components

Page Table Lookup

The system management or micro-kernel software tracks the mapping of pages from the program store in the level-3 memory to smaller level-2 memory. The number of entries used/required for this varies based on the Overlay Management Unit page size and the size of the level-2 memory. The Overlay Management Unit acts as a software-controlled cache into this page table, performs hardware address translation, and checks access permissions (Figure 3).

Two levels of cache are provided:

- The first level consists of micro TLBs (or µTLBs). These are very small, fully associative caches into the second level of the OLM cache. They allow for single-cycle translation and permission checking in the processor pipeline. The µTLBs are updated automatically from the second level of the cache.
- The second level of the cache is called the joint TLB (JTLB). This consists of a larger, RAM-based 4-way set-associative TLB. The JTLB is loaded by special kernel mode handlers known as TLB miss handlers.
- The final level of the hierarchy is the main page table itself. This contains the complete details of each page mapped for use by kernel or user tasks. The µTLBs, JTLB, and miss handlers combine to implement cached access into the OS page table.

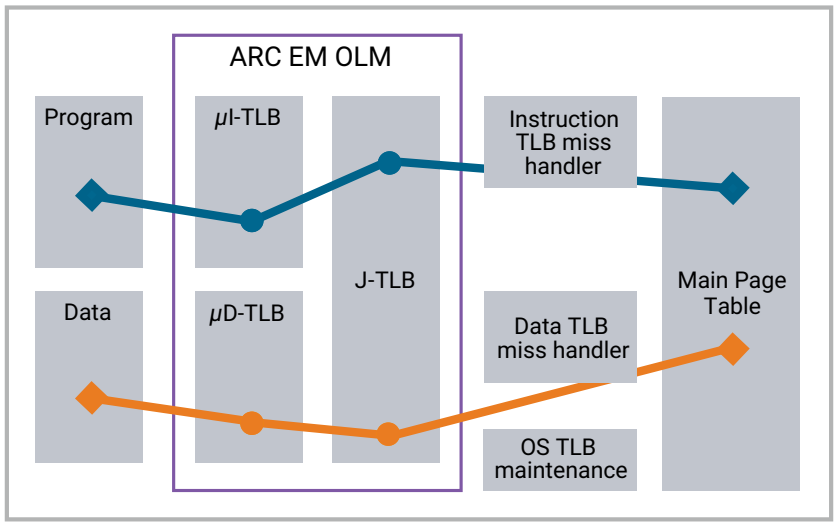

Figure 3: Overlay Manager Table Structure

Translation Lookaside Buffers

To provide fast translation from virtual to physical memory addresses the Overlay Management Unit contains Translation Lookaside Buffers (TLBs). The TLB architecture of the ARC EM's Overlay Management Unit can be thought of as a two level cache for page descriptors: "micro-TLBs" for instruction and data (μITLB & μDTLB) as level one, and the "Joint" (J-TLB) as level two. The μITLB and μDTLB contain copies of the content in the joint TLB. The μTLBs may have descriptors not contained in the joint TLB. In addition to providing address translation, the TLB system also provides cache control and memory protection features for individual pages.

The ARC EM implementation features a system configured as follows:

- The μITLB and μDTLB are fully associative and physically located alongside the instruction cache and data cache respectively, where they perform single-cycle virtual to physical address translation and permission checking. The μITLB and μDTLB are hardware managed. On a μITLB (or μDTLB) page miss, the hardware fetches the missing page mapping from the JTLB.
- The JTLB consists of a four-way set associative Joint Translation Lookaside Buffer with 64, 128 or 256 entries and is software managed. On a joint TLB page miss, special kernel-mode TLB miss handlers fetch the missing page descriptor from memory and store it in the JTLB, as well as swapping in the required contents from the main memory store into the level-2 memory. No part of the Overlay Management Unit has direct access to the main memory. The JTLB is filled by software through an auxiliary register interface.

Documentation

The following documentation is available for the DesignWare ARC Overlay Management Unit Option for ARC EM:

- ARCv2 ISA Programmers Reference Manual
- ARC EM Databook
- DesignWare ARC EM Integration Guide

Testing, Compliance, and Quality

Verification of the ARC EM Overlay Management Unit follows a bottom-up verification methodology from block-level through system-level. Each functional block within the product follows a functional, coverage-driven test plan. The plan includes testing for ARCv2 ISA compliance as well as state- and control-specific coverage points that have been exercised using constrained pseudo-random environments and a random instruction sequence generator

ARC EM Processors

The ARC EM processors, built on the ARCv2 instruction set architecture (ISA) are designed to meet the needs of next-generation system-on-chip (SoC) applications and enable the development of a full range of 32-bit processor cores – from low-end, extremely power-efficient embedded cores to very high-performance host solutions that are binary compatible and designed with common pipeline elements. ARC EM processors can be precisely targeted to meet the specific performance and power requirements for each instance on a SoC, while offering the same software programmer's model to simplify program development and task partitioning.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

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