SLM Path Margin Monitor

Measure timing margins of real functional paths In-Test or In-Field

Highlights

- Measures timing margin of actual functional paths In-Test or In-Field
- Granular delay elements for accurate measurement
- Each PMM unit can be shared with multiple functional paths
- Distributed architecture can handle 100's of PMM units with low overhead for scan
- Modes—Detection, Monitor, Toggle detect
- EDA integration for automated path selection, insertion, test pattern creation, and post silicon analytics
- Capture state of silicon precisely at any stage of its lifecycle and correlate with PVT monitors

Use Cases

- Silicon to Design Correlation
- Supply Margin Improvement
- In-Field Chip Performance Optimization
- Reliability Analysis

Overview

The Synopsys SLM Path Margin Monitor (PMM) solution consists of multiple PMM units, a PMM controller, and associated software and EDA automation. PMM IP is a building block for the PMM solution which is also supported by an automated implementation flow from Synopsys. Path selection logic, RTL configuration and generation, connecting to functional and/or test paths, synthesis, implementation, timing validation and path qualification are the key functions addressed by the EDA automation provided. Associated software allows the data generated from the PMM solution to be effectively analyzed and precise decisions made based on those insights.

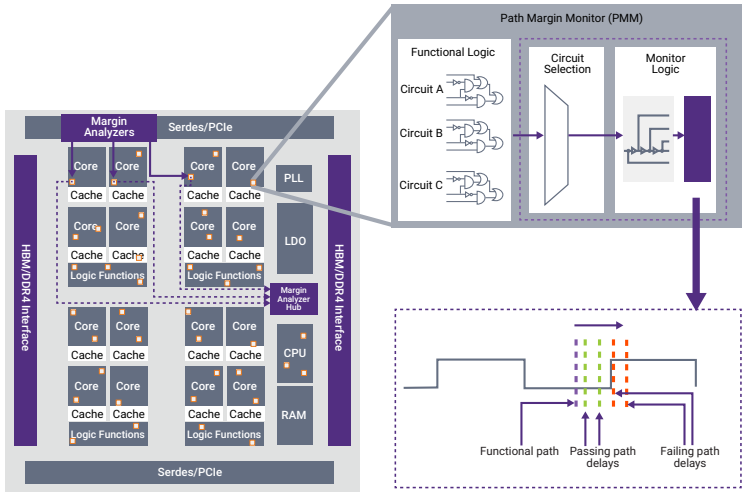

Figure 1: Path margin monitor solution

Path Margin Monitor Unit

The PMM unit (PMMU) enables timing margin measurement of a selected path in-test or during mission mode of operation. Timing margin is a key indicator of silicon structural health. Each PMM can handle multiple end points for measurement and each PMM controller can support multiple PMMs. On a single chip you can place hundreds of PMMUs with minimal area overhead, providing very valuable data which can be analyzed for insights to optimize any phase of silicon lifecycle. EDA and software automation along with path selection logic plays a crucial role in making PMMs practical.

Path Margin Monitor Controller

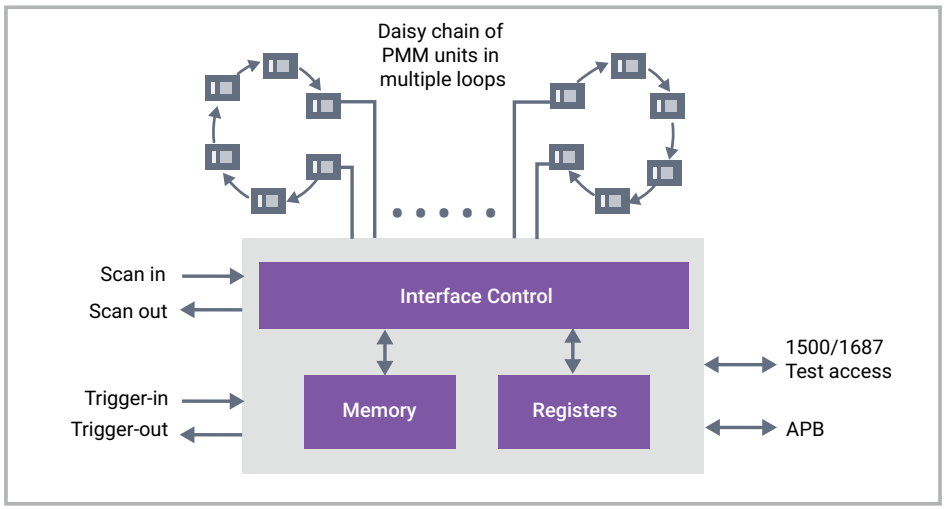

Figure 2: Path margin monitor controller

- Autonomous operation:
  - The PMM controller (PMMC) manages the configuration and data collection of the PMM units
  - Internal memory storage for configuration and results
- Supports multiple groups of PMM units based on power/clock/functional domains
- Provides first level data processing and filtering
  - Tracks number of failed PMM units
  - Compares results between consecutive runs
- Provides 1500/1687 and APB interfaces to connect to the test fabric or SoC functional fabric

Detection Mode:

- A sequence of measurement steps are performed to detect the longest path in the logic cone. Measurement is repeated periodically, and data is collected
- On chip processor analyzes the results to model margin delay across the chip

Monitor Mode:

- In this mode, the PMMU path delay muxes are programmed based on the margin model computed in the detection mode
- PM units continuously monitor the margin (pass/fail) to detect margin change
- When any of the monitors fail, data is collected and reported to the analytics subsystem

Toggle Detect Mode:

- In this mode, path monitors are configured to detect transitions in the selected path during a programmed period
- Periodic measurement produces data to build an activity model in various parts of the SOC. Toggle rate data can be used for aging and power management use cases

Key Features

- Fine grain delay elements for accurate measurement
- Distributed architecture with low overhead for scan
- Automated EDA flow for efficient implementation, data collection and analytics

Key Benefits

- Provides visibility of silicon structural health
- Real time reporting for analytics
- Monitor test or functional paths throughout silicon lifecycle
- Optimize silicon performance based on actual margins available

Complete Design Flow

Phase 1: DFT Tool

- Insert PMMU/PMMC and optionally DFT logic, connect to test fabric within the functional design

Phase 2: Digital Design Tool

- Synthesize, Scan stitching, P&R, CTS, connect PMMU to logic based on slack & proximity

Phase 3: STA & Margin Analysis Tool

- Validate the timing, extract path delay list, qualify selected paths

Phase 4: ATPG Tool

- Generate patterns to check operation of PMM units

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.

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