800G Ethernet PCS IP

Highlights

- Compliant with the IEEE 802.3 standard
- Configurable IP available in single or octal port
- Designed to be used with Synopsys 800G MAC IP for 800G Ethernet Systems
- Includes RS-FEC functions
- Supports IEEE 1588 standard
- Silicon proven
- Integration tested with the DesignWare 800G Ethernet MAC and 112G Ethernet PHY IP

Target Applications

- High-Performance Networking
- High-Performance Computing

Overview

The Synopsys 800G Ethernet Physical Coding Sublayer (PCS) IP, compliant with the 400G IEEE 802.3bs standard, provides a complete set of features enabling users to define an optimized PCS in products across a range of 800G Ethernet applications. The PCS IP implements two standard 400G PCS (IEEE P802.3bs) with bonding to create an aggregate 800G PCS.

The Synopsys 800G Ethernet PCS IP is available in single or octal port configurations. The IP in either configuration seamlessly interoperates with the Synopsys 112G Ethernet PHY IP.

The IP includes multiplexed Reed-Solomon Forward Error Correction (RS-FEC) functions for use by different channels at various speeds. The IP implements a 1024-bit wide CDMII for connections to the Synopsys MAC on the application side and 8-lane interface to the Synopsys PHY on the Ethernet line side.

Synopsys delivers a complete Ethernet solution with 800G Ethernet PCS IP, 800G Ethernet MAC IP and 112G Ethernet PHY IP.

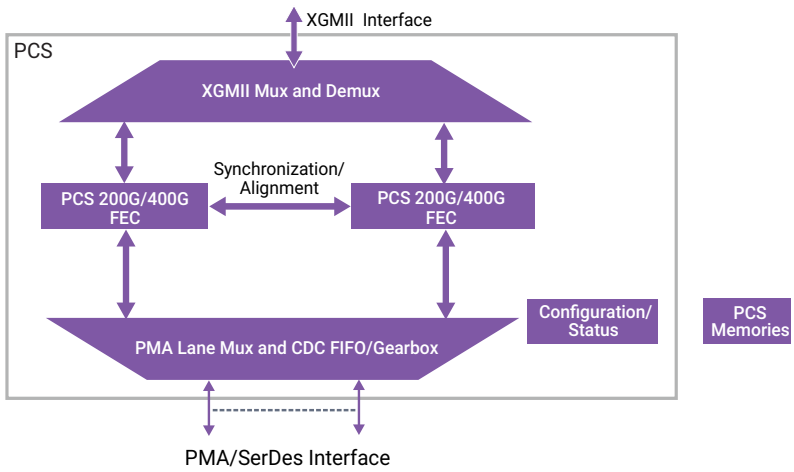

Figure 1: Synopsys 800G Ethernet PCS IP single port diagram

Key Features

- Common and single port features
  - 800G PCS implementing two bonded 400G PCS, which are IEEE P802.3bs compliant, create an aggregate 800G MAC interface
  - 8-lane 106Gbps SerDes interface with clock decoupling buffers and 1024-bit CDMII MAC interface when operating at 800G
  - Operation of 2x200Gbps
  - Programmable loopback on the SerDes interface available for application test
  - Transmit and receive data-path operating at 800MHz or higher common system clock
  - Direct 16/32-bit host interface to access configuration and status registers of the PCS, RS-FEC and RS-FEC extended statistics
  - MAC features supports IEEE 1588 1-step for 200G/400G and for 10G/100G
  - RS-FEC features supports RS-FEC implementing RS(528,514) and RS(544,514) and supports RS (272, 256) at least up to 100G
    - Supports 25G (Clause 108) and 50G (Clause 134) and 25/50G Ethernet consortium specifications
    - Supports IEEE802.3ck RS FEC codeword-interleaved (RS FEC Int, Clause 161) sublayer
    - Supports error indication to PCS when uncorrectable errors are detected
- Octal core features
  - Over 8x100Gbps SerDes (Proprietary), 400G over 8x50Gbps SerDes or 4x100Gbps SerDes, 200G over 4x50Gbps SerDes or 2x100Gbps SerDes
  - No support for 25G SerDes (16x25G, 8x25G)
  - Compliant with IEEE 802.3 Clause 82. 2x53Gbps or 1x106Gbps or 4x25Gbps (KR4) or 4x26.5Gbps (KP4)
  - 10G/25G/40G/50G layer compliant with IEEE 802.3 Clauses 49, 82, 107, 133, for 10G, 25G, 50G
    - Independent 64-bit XLGMII MAC interface per channel
    - Optional support for EEE fast-wake; No support for 40G (4x10G)
  - Non-required features that are removable for optimizations: Base-R (Firecode) FEC and EEE (Energy-Efficient Ethernet)
  - Multi-rate/multichannel features
    - Up to 8 channels independently usable for 10G or 25G or 50G or 100G Ethernet single-lane applications
    - Up to 4 50G Ethernet channels using two 25Gbps lanes each
    - Up to 2 100G Ethernet channels using four 25Gbps lanes each
    - Up to 4 100G Ethernet channels using two 50Gbps lanes each
    - Up to 2 200G Ethernet channels using two 50Gbps lanes each
    - Up to 4 200G Ethernet channels using two 100Gbps lanes each
    - Up to 2 400G Ethernet channels using two 100Gbps lanes each
    - One 400G Ethernet channel using eight 50Gbps lanes
    - One 800G Ethernet channel using eight 100Gbps lanes

Deliverables

- SystemVerilog RTL Source code
- Verilog Testbench environment with example testcases
- Scripts and constraints files for implementation tools like Spyglass Lint/CDC, DesignCompiler, etc.
- IPXACT views for register maps

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.

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