

# Accelerating 20nm Double Patterning Verification with IC Validator

## Author Abstract

**Paul Friedberg**  
Corporate  
Applications  
Engineering

**Stelios Diamantidis**  
Product Marketing

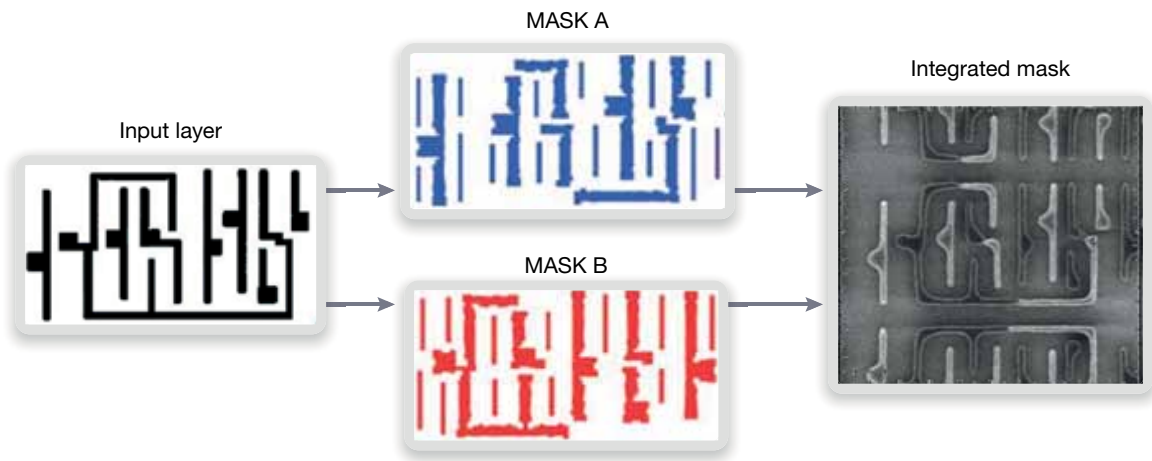
The emergence of Double Patterning Technology (DPT) for 20nm lithographic printability represents the single most significant design challenge for manufacturing since computational lithography enabled scaling below the 193nm illumination wavelength. DPT introduces new considerations in every step of the design flow; including floorplanning, placement, routing, extraction, and physical signoff verification. This whitepaper presents the key concepts of DPT compliant design and demonstrates how new signoff technology in IC Validator makes it possible to ensure 20nm manufacturing compliance. Recognizing that the designer productivity necessary cannot be achieved alone by point-tool enhancements and post-processing techniques, the paper outlines advances in In-Design physical verification within IC Compiler. Smart integration enables automated detection and correction of non DPT-compliant design geometries, eliminating wasteful iterations and accelerating design closure for manufacturing.

## Introduction

A wealth of patterning enhancements and computational lithography techniques — immersion, off-axis illumination, phase shift masks, sub-resolution assist features, optical proximity correction, and more — have allowed 193nm-based photolithographic resolution scaling down to roughly an 80nm pitch. At the 20nm node, Moore's Law scaling calls for 64nm pitch on 1x metal routing layers. However, the combined power of all advanced lithographic techniques still falls short of meeting this minimum resolution requirement with a single exposure. Next-generation photolithography using 13nm extreme ultra violet (EUV) light sources will not be available or economical for large-scale production of 20nm (and likely sub-20nm) integrated circuits (IC).

To continue to enable Moore's law past 28nm using existing 193nm wavelength illumination, the semiconductor industry will rely upon double patterning technology. DPT allows lithographers to effectively double the feature frequency on wafer and thereby achieve 20nm node imaging requirements. This is made possible by dividing alternating layout geometries onto two masks and patterning with two sequential exposures, using an etch step between exposures to isolate the separate images.

DPT represents a breakthrough in patterning technology on the manufacturing side but not without imposing new, significant restrictions on the design side. The key enabler for DPT is the ability to ensure that the drawn layout can be legally decomposed onto two masks (see Figure 1). This procedure, which is commonly referred to as color decomposition, relies on a new set of design rules that apply to the color-decomposed layout. These rules encapsulate the fundamental photolithographic limitations and prohibit two polygons of the same color from having a particular geometric relationship.



**Figure 1: Double patterning decomposition. An input design layer is split into 2 masks to overcome fundamental photolithographic limitations.**

The impact of DPT on physical designers is two-pronged. First, on the implementation side, the new rules need to be actively taken into account during placement and routing. Costs associated with the decomposability problem need to be considered alongside the existing costs (timing, area, etc.) to find an optimized design solution. Second, on the physical verification side, a signoff-quality coloring process must be able to confirm that a legal mask decomposition solution exists for the entire design, using the exact specifications in the foundry's design rule manual (DRM). In addition, these new requirements need to be addressed with no impact to designer productivity and overall design turnaround time. The stakes are high: Any single DPT violation left behind will render the design unprintable and can lead to missed tapeout and market opportunity windows. The challenges and solutions for DPT compliance addressed by physical verification with IC Validator will be covered in the rest of the paper.

## IC Validator Double Patterning Signoff Technology

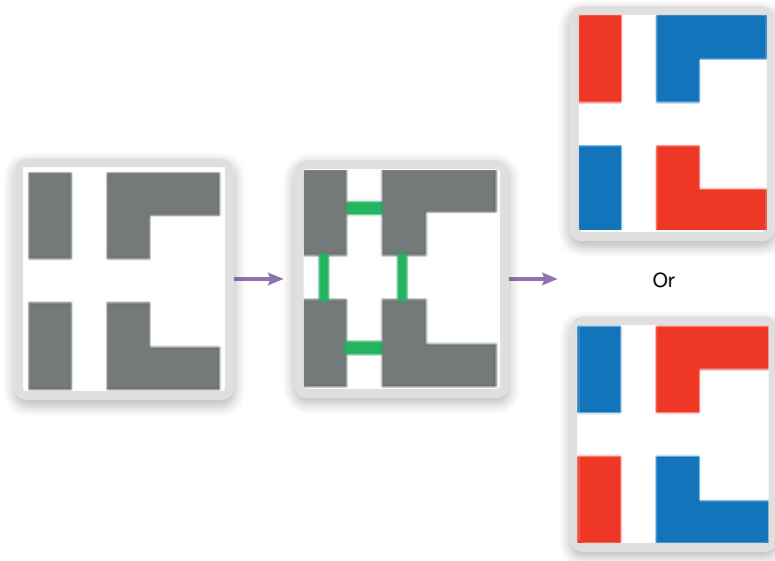
The principal core technologies required for signoff-quality DPT color decomposition are (1) the ability to formulate advanced rules and (2) synthesize those rules with a coloring engine to analyze the decomposability of a layout.

### Formulating Advanced Rules

DPT rules provide the crucial foundation of DPT decomposition. By capturing these rules accurately, the coloring problem is reduced to its essential elements: series of DPT polygon "cycles" whose components must be decomposed into alternating colors, with the only alternate solution being the reverse color assignment of the entire cycle.

IC Validator's dual polygon- and edge- based processing engine enables the user to define very complex geometric rule requirements. New rules created for DPT generally dictate minimum spacing between polygon edges and corners of facing sides or line ends that are assigned to the same mask. When applied on a target design, they capture relationships between polygons and edges that DPT rules dictate must reside on separate colors. In some cases, more elaborate rules can be used to enable "stitching" of geometries. Stitching allows for a single polygon to be subdivided into two masks, so that one edge of the polygon is assigned the first color while another edge is assigned the second color.

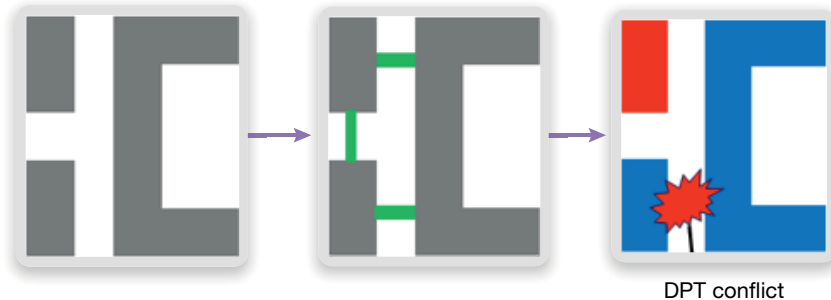
In addition, the flexible nature of IC Validator's PXL programming language is essential for enabling accurate specification and rapid customization of the decomposition flow. Instead of overloading the tool's geometry engine with rigid capabilities to enable stitching, color balancing or hierarchy prevention, IC Validator makes it possible for users to access and configure decomposition directly through PXL. This enables foundries to optimize implementation not just on tool capabilities and requirements, but also desired use model and performance.



**Figure 2: Basic decomposition approach — identify coloring-critical spacing relationships, then apply decomposition engine.**

### Analyzing Decomposability of a Layout

To assign a coloring solution, IC Validator offers a native, hierarchical coloring engine that is fully integrated into the physical verification framework. The engine consumes the uncolored input design and color-critical relationships between various polygons (DPT polygon cycles), and decomposes all layout geometries into two colors (see Figure 2). Whenever the decomposition encounters a scenario where two polygons must be colored the same color (a scenario termed a DPT “odd-cycle”), coloring assignments are made and a DPT violation is reported to the user.



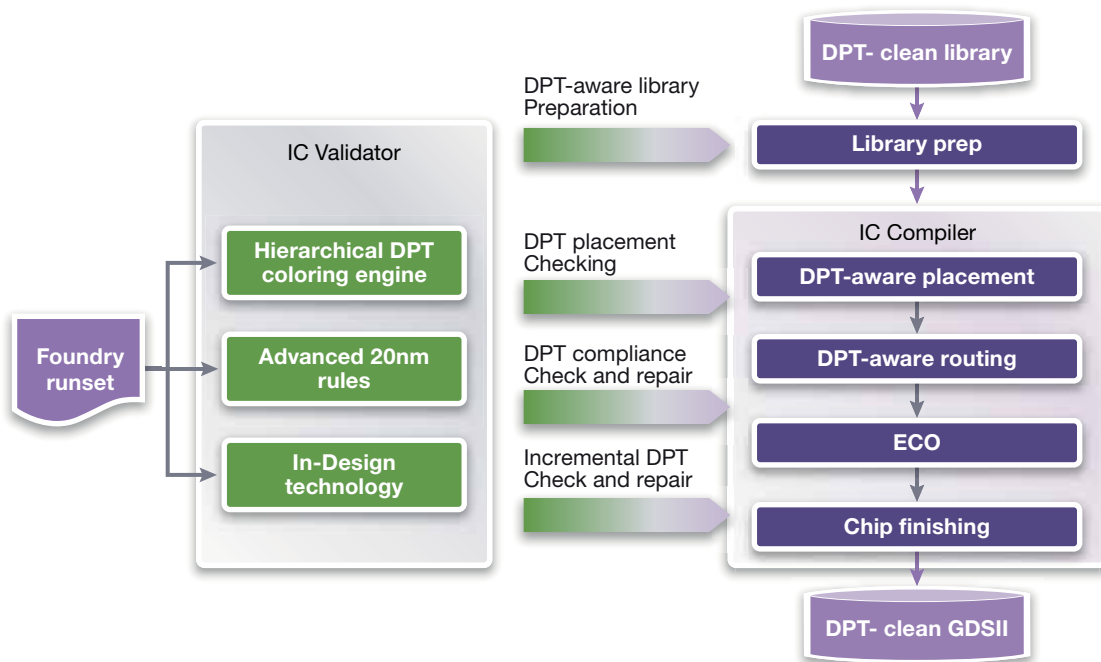
**Figure 3: DPT odd-cycle gives rise to a decomposition conflict.**

Since IC Validator returns the color-decomposed design to the user, any DPT conflicts can be observed with color assignments in place (see Figure 3). This is a critical attribute as it enables the designer to run through iterative debug of DPT conflicts in tandem with standard DRC errors, and also downstream design tools to consume IC Validator’s coloring output for further analysis.

In many cases, the color-critical relationships span multiple levels of design hierarchy. IC Validator’s color engine intelligently manages hierarchy, exploding geometries only to the necessary level in hierarchy to complete the color assignments, and then pushing instances back to lower levels wherever possible. Hierarchical processing ensures signoff quality analysis with best possible performance, accelerating design turnaround time.

### IC Validator In-Design Technology for DPT with IC Compiler

With an efficient coloring engine integrated alongside standard capabilities for capture of complex design rules, IC Validator can be deployed throughout the design flow to optimize management of DPT requirements and to ensure DPT compliance.



**Figure 4: Flow diagram for DPT-aware design. IC Validator DPT-aware library preparation is used to seed DPT-aware placement; IC Validator's DPT compliance checking is invoked throughout the routing sequence to ensure a DPT-clean result.**

### DPT-aware Placement

There are multiple levels of consideration for DPT-aware library preparation. IC Validator addresses both levels of library preparation by offering compliance checking with consumable coloring information.

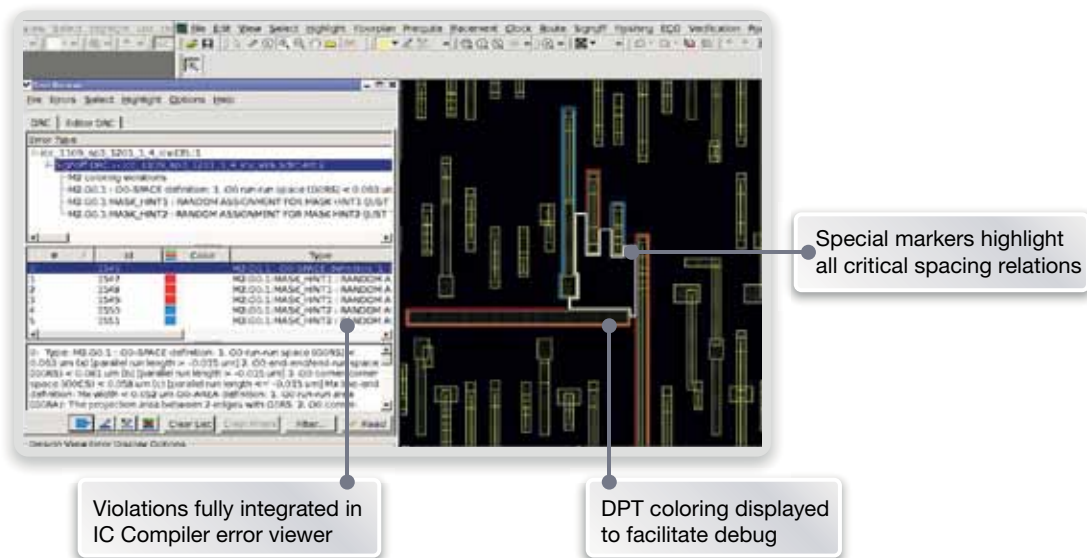
At the base level, the cell designer must ensure that the drawn layout can be safely decomposed into two colors — *intra-cell* conflicts must be resolved before a cell can be signed off as DPT-clean. IC Validator can be used to create preliminary coloring assignments within each standard cell in a given library. In case a violation is detected, targeted feedback is provided to the designer in the event of unresolved internal DPT conflict.

At the higher level, cell design should consider the downstream placement implications of how polygon coloring assignments from one cell will interact with coloring assignments at the edge of an adjacent cell — inter-cell DPT conflicts may arise if cell-to-cell spacing is insufficient. A conservative approach during placement would apply a blanket heuristic to enforce extra spacing between all neighboring cells. In many cases, however, cells can safely abut without allowing extra space due to the arrangement of data polygons. IC Compiler's placer engine can consume IC Validator's coloring information to manage optimal DPT-aware placement (see Figure 4).

### On-demand DPT Compliance Checking

At any step in the physical design process, IC Validator can be invoked In-Design to confirm that the design under construction conforms to foundry 20nm DRC and DPT rules. IC Compiler's placer and router engines feature DPT-aware technology that offers a correct-by-construction to DPT design. Yet designers are finding that there are still plenty of moving parts in the design process that can lead to violations and late-stage surprises — such as technology file mismatches, stale IP abstractions, and very long range cycles.

To enable earlier and localized identification of DPT violations, IC Validator is integrated with IC Compiler using In-Design technology, and offers on-demand DPT compliance checking. This flow is based on IC Validator's DPT signoff decomposition checking technology, as described in the previous section of this paper, to perform on-the-fly identification of critical DPT spacing relationships and fast coloring analysis for conflict detection (see Figure 5).



**Figure 5: In-Design technology for on-demand DPT decomposition checking; enables earlier detection and faster debug of DPT violations.**

In-Design technology integration offers the ability to launch layout decomposition analysis within the IC Compiler cockpit; tracking of violations and context in the IC Compiler error viewer; special marker visualization to highlight all shapes participating in a DPT violation; and DPT coloring displays to facilitate comprehension and debug. All functionality is performed natively, directly on the underlying design database, eliminating the need for large file streaming, unfamiliar tool setup, and error prone translation steps.

### Automatic DPT Repair

To accelerate manufacturing closure at 20nm, IC Validator offers new In-Design technology with IC Compiler to automate the process of DPT repair. Traditionally, designers have relied on post-route manual fixes to resolve DRC violations. However, DPT violations can be significantly more difficult to resolve, requiring expert engineers and unpredictable fix-verify iterations (also see Case Study 2, below).

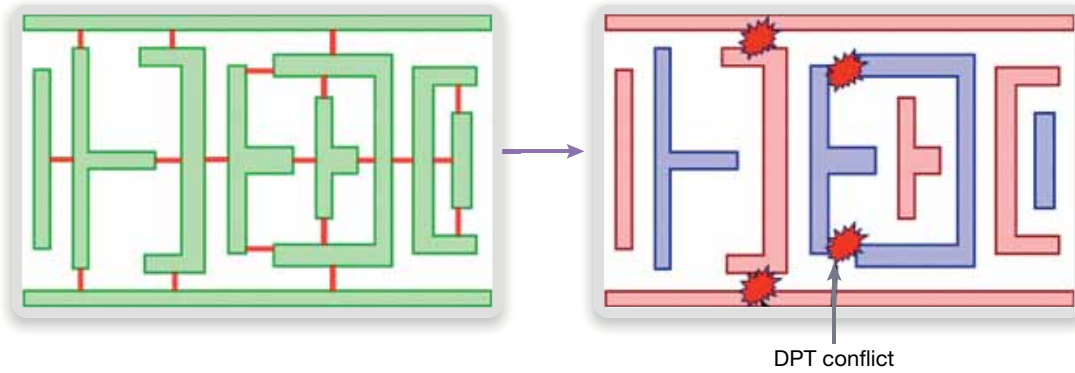
IC Validator addresses the problem of DPT repair in a holistic and fully automated fashion. Once on-demand decomposition analysis has been completed and a violation has been detected, graph analysis is performed to identify the odd-cycle properties and track participating geometries. Opportunities for repair are then generated and prioritized using cost-driven analysis, in a manner similar to IC Compiler Zroute's violation prevention technology. Finally, IC Validator guides the router through the repair queue, a heuristic-driven approach that maintains natural design evolution to final signoff, eliminating manual fixes and saving designers hours of tedious and error prone work.

## Case Studies

IC Validator DPT functionality is already being used in development of 20nm production flows. In this section, we will explore two case studies. First, we will see how IC Validator is used at cell level for library preparation in advance of DPT-aware placement. Second, we will offer an example of IC Validator's on-demand DPT compliance checking and repair during routing.

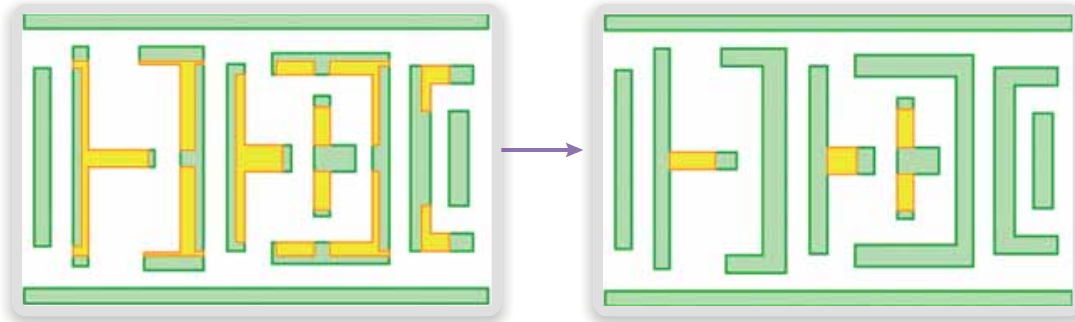
### Case 1: DPT-aware Library Prep and Placement

In an example 20nm cell library, the designer has created an XOR gate and would like to determine whether the design is decomposable and evaluate its placement properties. By invoking IC Validator's cell-level DPT analysis, the cell is first decomposed according to a baseline set of cell conditions: both power rails must be assigned to the same color and no polygons may be stitched. As shown in Figure 6, this results in DPT conflicts.



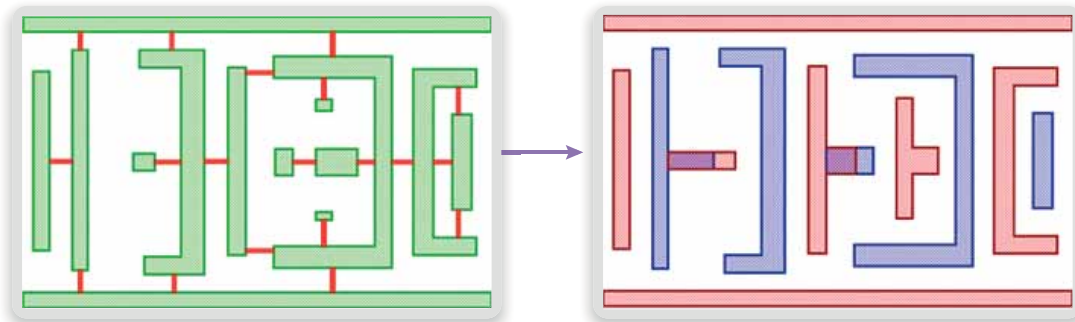
**Figure 6: First stage of cell-level coloring. DPT-critical relationships are established between polygons (left), and color decomposition is invoked (right). Conflicts are present.**

The process in question does allow stitching within polygons, so IC Validator can make a second pass to attempt to resolve DPT conflicts with a more sophisticated decomposition (see Figure 7). Raw areas that are safe to be used for stitching are determined based on color spacing rules, and are then further whittled down into areas that are fully legal to use for stitching according to color overlap rules.



**Figure 7: Second stage of cell-level coloring. All sub-regions of polygons that are not strictly DPT-critical are marked (left), and then legalized according to overlap rules (right)**

Finally, the legal stitching regions are temporarily removed from the design and IC Validator proceeds with decomposition of the color-critical regions. After reinserting those stitching regions and assigning colors based on the local context, the cell has been safely decomposed as shown in Figure 8.



**Figure 8: Final stage of cell-level coloring. Candidate stitching regions are removed from the coloring-critical problem (left), and IC Validator colors the critical areas and evaluates candidate stitching regions accordingly (right).**

The characterized cell can now be readily consumed during DPT-aware placement to ensure maximum cell density with guaranteed zero DPT conflicts.



## Case 2: In-Design Technology for On-Demand DPT Compliance Checking and Automatic Repair

IC Validator can be very effective when it comes to identifying and addressing 20nm DPT corner-case violations. In this customer case, an M3 odd-cycle is identified as part of a timing ECO loop (see Figure 9).

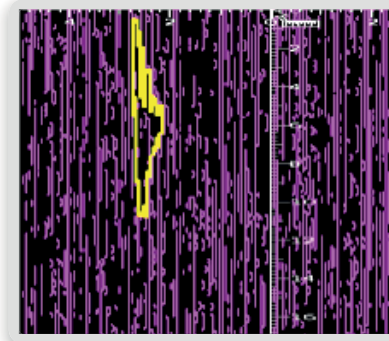


Figure 9: A long-range DPT violation on M3

The cycle seems relatively benign, involving approx. 25 shapes and offering multiple apparent opportunities to adjust shapes in order to break it. The designer attempts a fix in the lower part of the cycle; two neighboring shapes in the cycle can be separated by sufficient distance to break the associated DPT link, and the odd-cycle is expected to be resolved. A subsequent block-level decomposition check, however, reveals that the cycle has actually expanded into a broader cycle that “nested” the original, smaller cycle (see Figure 10).

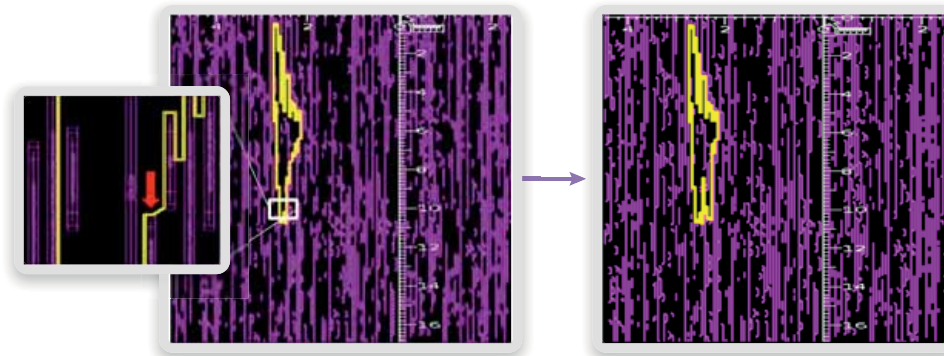


Figure 10: Manually repairing a DPT violation — attempted fix #1

The designer decides to attempt a second fix, selecting another line-end that can be safely pulled back to successfully break the DPT link with a neighboring shape. The DPT odd-cycle is expected to be broken once again. A 3rd pass at decomposition checking reveals yet another nesting odd cycle, this time involving approx. 50 shapes (see Figure 11). The designer is now facing the predicament of attempting another lengthy fix-then-verify loop.

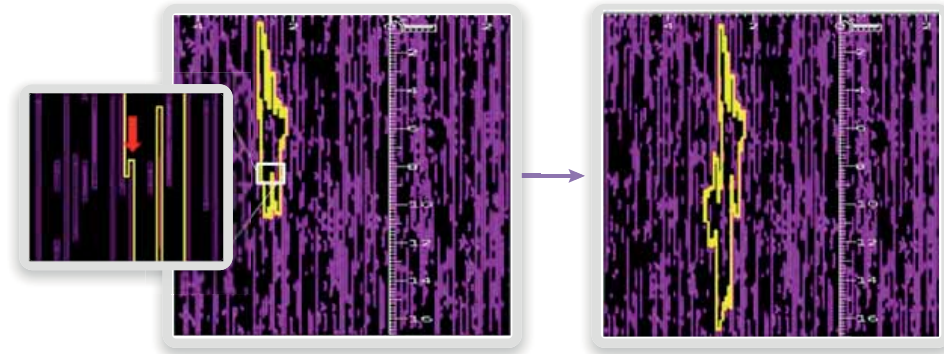
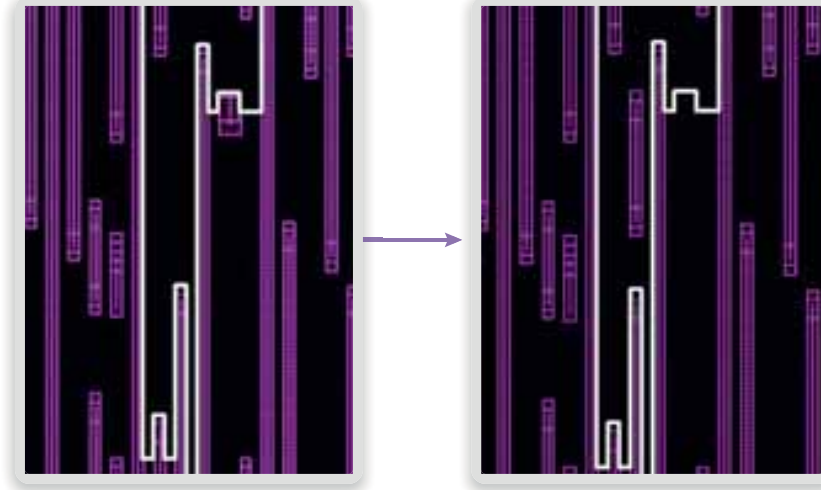


Figure 11: Manually repairing a DPT violation — attempted fix #2

Recognizing that the productivity needed for 20nm design can only be achieved through flow-level improvements, IC Validator offers automatic DPT repair (ADR) for faster manufacturing closure.



**Figure 12: DPT ADR — automatically repairing a DPT violation**

As seen in Figure 12, IC Validator ADR identifies a critical link in the original odd cycle shown in Figure 10, and relocates only a single shape to break that link and fix the odd cycle without causing any new, nested cycle to result. This repair is unlikely to have been envisioned by human inspection, and, due to the high routing congestion in the region, alternative repairs are unlikely to have fully corrected the decomposition conflict. By contrast, the repair achieved by ADR not only resolves the DPT violation, but is DRC-clean, minimally invasive from physical standpoint, and causes no degradation to timing. Within minutes, the design is healthy and tapeout is back on schedule.

## Summary

At the 20nm node, double patterning lithography introduces new requirements on physical verification to ensure layout decomposability. IC Validator offers cell-level color decomposition during library preparation (seeding DPT-aware placement) as well as In-Design DPT compliance check and repair within IC Compiler. With the available suite of IC Validator's DPT technologies, designers can minimize late-stage manual fixes and design iterations related to double patterning, accelerating overall design closure for manufacturing

IC Validator DPT technology offers:

- ▶ Signoff-quality DPT compliance checking
- ▶ DPT error visualization in multiple designer-friendly formats
- ▶ In-Design technology for DPT-aware placement and on-demand compliance checking within IC Compiler
- ▶ Automatic router-driven DPT repair with minimal physical/timing impact
- ▶ Advanced manufacturing flows for DPT aware density management, extraction, and pattern matching
- ▶ Push-button ease of use

To find out more about Synopsys and IC Validator, visit <http://www.synopsys.com/icvalidator>.