SYNOPSYS®
Predictable Success

Synopsys and Progate Group

Formality increases designer productivity with faster runtimes

Meeting the tapeout schedule is critical in the turnkey design services business. Formality® successfully verified our datapath-intensive wireless LAN design in one-fifth the time. DC Ultra and Formality are a winning combination for meeting our performance goals in the shortest possible time."

Jasper Lee
Technical Design Manager, Progate Group Corporation

Business

Progate Group Corporation (PGC) was the first turnkey design services business in Taiwan and has successfully taped out more than 900 designs since the company was founded in 1991. PGC serves the industrial automation, automotive electronics, aerospace, RF, security and storage industries.

Challenges

- Attaining aggressive performance goals
- Meeting strict customer tapeout deadlines

Solution

- Design Compiler® Ultra for synthesis
- Formality for equivalence checking
- IC Compiler for layout

Benefits

- Significant time savings in verifying datapath-intensive designs
- Predictable results
- Simplified design flow
- Simple, straightforward setup

Overview

Design process predictability and delivery to the committed schedule are key elements to the success of the turnkey design services business at PGC. Because PGC's designs are datapath-intensive, its engineers need the full power of DC Ultra to concurrently optimize timing, area, and power while achieving high correlation between synthesis and place and route.

But DC Ultra's complex optimizations can pose a significant challenge to traditional equivalence checking (EC) tools. With PGC's previous EC tool, designers had experienced excessive runtimes that required weeks to complete. Making any last-minute changes to a design could have delayed its tapeout schedule.

"We were spending a great deal of time and effort trying to get equivalence checking to pass in our designs." said Jasper Lee, Technical Design Manager, at PGC. "Due to our aggressive schedules, we could not afford to wait weeks for equivalence checking to complete."

The combination of DC Ultra and Formality has helped us achieve our aggressive timing and area goals and create designs that are fully verifiable. Formality has shaved weeks off our schedules and helped us tapeout our chips with confidence."

Jasper Lee
Technical Design Manager, Progate Group Corporation

A winning strategy

By using Formality to verify the wireless LAN design, engineers at PGC were able to take advantage of all the advanced timing, area, and power optimizations in DC Ultra to meet their challenging performance goals.

Formality recognizes and verifies the complex optimizations applied in DC Ultra such as datapath optimizations, full chip phase inversion, and retiming. These optimizations provide key timing and area benefits that are fully verifiable with Formality.

"Formality required minimal setup, is easy to use, and easily fit in our existing flow," said Jasper Lee, Technical Design Manager, at PGC. "Formality has been successfully used by designers of all levels of experience at PCG."

Key competitive advantage

Because Formality was easy to implement and compatible with PGC's design flow with DC Ultra, Formality is now being used on all design projects. Formality is helping the designers achieve full chip verification with higher quality-of-results in less time.

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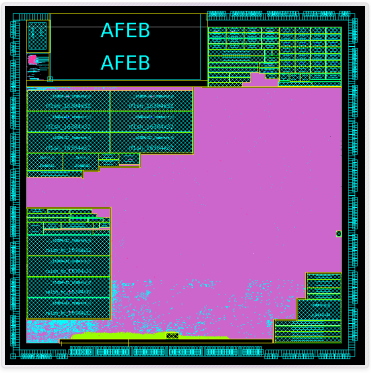
PGC is using DC Ultra and Formality on all of their designs. The combination of DC Ultra and Formality has helped PGC achieve high levels of performance in a quick product development cycle which are key competitive advantages.



"Formality is easy to setup and use. The auto setup feature in Formality enables a very high first pass success rate."

Jasper Lee
Technical Design Manager, Progate Group Corporation

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