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Synopsys and LG Electronics

DFT MAX compression and TetraMAX ATPG enable higher-quality testing at LG Electronics

"Using DFT MAX compression to reduce test data volume for our new HDTV chip allowed us to apply all the test patterns at one time and take full advantage of the higher test quality possible with DSM tests."

Woo-Hyun Paik
Research Fellow, LG's System IC Business Team

LG Electronics

Business

LG Electronics, Inc. is a global leader and technology innovator in consumer electronics, home appliances, and mobile communications.

Challenges

- Meeting stringent deep submicron (DSM) defect screening goals
- Reducing the cost of high-quality testing
- Implementing test compression without impacting design schedules

Solution

- DFT MAX compression to reduce test data volume and test time
- TetraMAX® ATPG for DSM test pattern generation
- PrimeTime® static timing analysis for high-quality at-speed patterns

Benefits

- Higher test quality than previously possible
- Lower cost of defect screening
- No impact on tapeout schedules

Overview

The System IC Business Team at LG Electronics, Inc. (LG) produces high-definition television (HDTV) and mobile TV chip sets for LG TV and handheld equipment manufacturers worldwide. Timely delivery of defect-free products to its customers is essential to LG's success in this highly competitive market. Consequently, LG has developed stringent deep submicron (DSM) defect screening goals for its products. One of the company's key challenges is meeting its product quality objectives while still maintaining tight control of project schedules and testing costs.

To meet LG's strict defect screening goals for the latest HDTV product, engineers in the System IC Business Team needed to generate more types of DSM tests than had been required for the previous generation of designs. The demand for additional DSM tests was driven by the complexity of the design, which consisted of approximately 2.3 million instances and 400,000 scan flops, and the fact that it would be fabricated in a 65-nanometer manufacturing process.

We outsource much of our production testing to specialty firms that use low-cost ATEs. Without scan compression, only a fraction of our DSM test patterns can be loaded at one time on these testers, and reloading patterns into memory during full-scale production testing is costly in terms of both time and money."

Woo-Hyun Paik
Research Fellow, LG's System IC Business Team

Nanometer test challenges

At these integration levels, manufacturing process variations introduce defects that are too subtle to detect using conventional ATPG tests. For example, "small delay defects" contribute to delays much smaller than the clock cycle time, and these additional delays can cause device failures. While standard transition delay ATPG is not effective detecting these small delay defects, Synopsys' TetraMAX Automatic Test Pattern Generation (ATPG) can explicitly target them using accurate timing information about the design to guide pattern generation. TetraMAX ATPG directly accesses the information it needs from PrimeTime static timing analysis, the industry's de-facto signoff solution.

Using standard scan testing, the application of all the DSM tests—transition-delay, bridging, and small delay defect tests—would have substantially increased the total number of test patterns. The resulting inflation in both total pattern count and test data volume per pattern, while dramatically boosting defect coverage for the design, would have made it impossible to load all the patterns into automatic test equipment (ATE) memory, creating a formidable bottleneck in production screening.

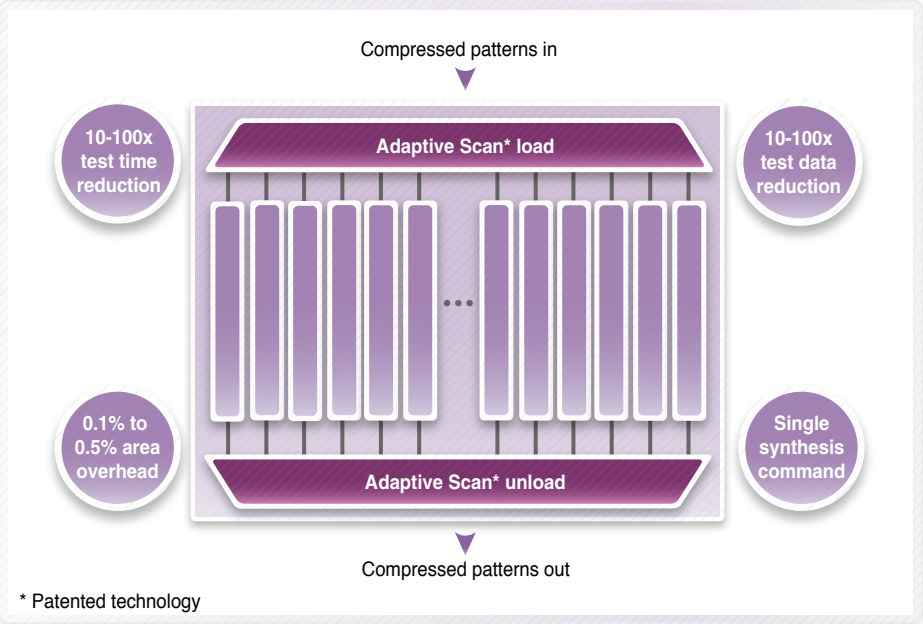
"We outsource much of our production testing to specialty firms that use low-cost ATEs," said Woo-Hyun Paik, Research Fellow at LG's System IC Business Team. "Without scan compression, only a fraction of our DSM test patterns can be loaded at one time on these testers, and reloading patterns into memory during full-scale production testing is costly in terms of both time and money."

Higher test quality enabled by compression

To enable higher-quality testing, the LG engineers implemented DFT MAX compression on the new HDTV design. Working seamlessly within Synopsys' Galaxy™ Implementation Platform, DFT MAX compression synthesizes compression on-chip to substantially reduce test data volume and test application time. Its patented Adaptive Scan technology produces predictable compression results with virtually no impact on timing.

"Using DFT MAX compression to reduce test data volume for our new HDTV chip allowed us to apply all the test patterns at one time and take full advantage of the higher test quality possible with DSM tests," said Woo-Hyun Paik, Research Fellow at LG's System IC Business Team.

The deployment resulted in first-silicon success that enabled high-volume, cost-effective production testing of the HDTV chip that met LG's quality goals without the need for costly investments in ATE infrastructure.



DFT MAX compression

A winning strategy

LG is now implementing DFT MAX compression on all its TV chip sets. The product's ease-of-use and compatibility with LG's existing design flow that includes Design Compiler®, PrimeTime, and IC Compiler has enabled the engineers to rapidly deploy the solution on more than ten multi-million-gate designs.

Voyager Mobile Phone: Demo product using LG's ATSC M/H baseband chip featured at the 2009 International Consumer Electronics Show

"Synopsys' DFT MAX compression requires very little design effort to achieve predictable compression results, and does not impact our tapeout schedules. Our engineers are using it successfully on our complex designs to reduce the cost of meeting LG's high-quality goals."

Woo-Hyun Paik
Research Fellow, LG's System IC Business Team

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Synopsys, Inc. • 700 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

04/09.CE.09-17121.