SYNOPSYS®
Predictable Success

Synopsys and PLX Technology

DC Ultra delivers superior performance with higher predictability for PLX Technology

We see on average 10-15% superior performance with DC Ultra. Its topographical technology predicts results that are within 5% of post layout results cutting weeks off of our implementation time. Superior performance with higher predictability is what drives us to use DC Ultra for all our synthesis needs."

Syed Ahmed
Engineering Director, PLX Technology

Business

PLX Technology, Inc., the leading global supplier of PCI Express (PCIe®) switch and bridge silicon, recently announced four new high performance PCIe switches targeting servers, enterprise storage, control planes, and ultra-gaming, while featuring the highest PCIe switch lane counts in the industry. PLX is the market leader in PCIe switches and is the only supplier with 96 lane and 80 lane options, as well as x16 support which is critical for designers requiring the highest levels of performance and throughput, such as graphics and backplanes.

The new PLX ExpressLane™ PEX 8696 (96 lanes, 24 ports), PEX 8680 (80 lanes, 20 ports), PEX 8664 (64 lanes, 16 ports) and PEX 8649 (48 lanes, 12 ports) are PCI-SIG® PCIe 2.0 (Gen 2) specification-compliant switches with distinguishing PLX-only features, including support for x16 port configurations and non-transparency (NT), as well as visionPAK™ and performancePAK™ development tools. The new PLX devices also implement game-changing Multi-root and Multicast features. These large switches allow designers to build switch fabrics, redundant backplanes and large IO/storage drawers without having to deal with high latency, high power consumption and bandwidth limitations associated with use of multiple smaller switch chips.

Challenges

- Schedule predictability
- Meet stringent performance/area/power design goals

Solution

- DC Ultra™ with Topographical Technology

Benefits

- Synthesis results correlate to layout eliminating time-consuming iterations between synthesis and layout
- Easy to adopt
- DC Ultra's advanced optimizations for best-in-class timing, area, and power results

Overview

As the global supplier of PCI Express (PCIe®) switch and bridge silicon, PLX designers are challenged to meet the stringent performance targets with-in time-to-market window. PLX designers were experiencing miss-correlation between synthesis results and layout results using their traditional wire-load model

based synthesis. Performance results seen after RTL synthesis did not match with the results seen after layout and in many cases designers needed to modify their RTL source and re-synthesize the designs to meet the performance targets. These iterations between synthesis and layout impacted their schedule adversely. RTL designers needed a synthesis solution that enabled them to foresee layout results and provides a starting point that can meet their performance targets.

Solution – DC Ultra

DC Ultra is the best-in-class, RTL synthesis solution that concurrently optimizes for timing, area, power, and test targets. It includes many sophisticated synthesis optimization techniques such as advanced data path synthesis, register retiming, critical path re-synthesis, and intelligent constant register removal to deliver superior quality of results.

DC Ultra offers multicore support for fast runtimes, using advanced parallel and threaded capabilities to maximize efficiency. By utilizing the advanced synthesis optimizations of DC Ultra, designers at PLX were successful in meeting their design's timing targets.

DC Ultra includes topographical technology that utilizes Synopsys' best-in-class placement and optimization technologies to drive accurate interconnect delays. This allows DC Ultra to accurately predict post-layout design results such as timing, power, and area during synthesis.

Topographical technology also utilizes clock tree synthesis technology to estimate post-layout power consumption of the design. Topographical technology is designed for RTL designers and requires no physical design expertise or changes to the synthesis use model. By deploying DC Ultra with topographical technology, RTL designers at PLX were able to accurately predict design's quality of results such as timing, area and power consumption at synthesis stage. This accuracy of results allows them to identify and fix design issues while still in synthesis to create a better start for physical implementation.

"DC Ultra cuts weeks off of our project schedule by reducing time-consuming iterations previously required between synthesis and layout to close on design goals", said Syed Ahmed, Engineering Director, PLX Technology. "It improves time to results by driving a convergent RTL to GDSII flow. And with DC ultra's advanced synthesis optimizations we achieved 15% better timing results compared to our previous synthesis solution."

A Winning Strategy

PLX is using DC Ultra with topographical technology on all of their designs. Synopsys' DC Ultra helped their designers achieve superior results with higher predictability and accelerate their design cycle which is essential for PLX's success.

"Tight correlation between synthesis and layout results is critical to minimizing iterations in our design flow. With DC Ultra topographical technology we are able to provide a better starting point to place and route, streamline our implementation flow and cut about 3 weeks off of our project schedule."

Syed Ahmed
Engineering Director, PLX Technology

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