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WHITE PAPER

Eliminate Chip-killing Bugs with Power-Aware RTL CDC Verification

Authors

Deepak Ahuja
R&D Engineer, Principal

Navneet Chaurasia
Sr Applications Engineer

Overview

System on Chip (SoC) complexity continues to grow as semiconductor companies aim to introduce new functionality, which is driving dramatic growth in design size. Chips are increasingly using low power techniques such as power switches, isolation cells, retention cells, and level shifters to reduce power consumption. Designers are implementing IPs at different voltages to reduce switching power, thereby, minimizing overall power consumption. Generally, these power cells are introduced late in the design cycle potentially breaking pre-qualified paths, introducing metastability, glitch, and convergence problems resulting in chip-killing bugs. This highlights the need for a powerful methodology during the early RTL stage to ensure that the new low-power logic introduced in the design doesn't introduce any bugs during later design stages.

This white paper provides some background on UPF-aware clock domain crossing challenges and outlines VC SpyGlass CDC UPF-aware methodology that can help catch bugs otherwise detected at later design stages and provide consistent behavior across low-power verification as well as implementation flows, resulting in reduced iterations.

CDC Challenges for Low-Power Designs

Low-power design techniques are used widely to enable advanced power-management strategies in complex SoC designs. Using clock logic to operate the chip at high frequency and to turn off some portions of the SoC when inactive to reduce power consumption is common. It is imperative for power management techniques to be added to the design to reduce power consumption without impacting functionality (refer to figure 1). Such techniques also help reduce static and dynamic power consumption allowing more functionality to fit onto a smaller chip.

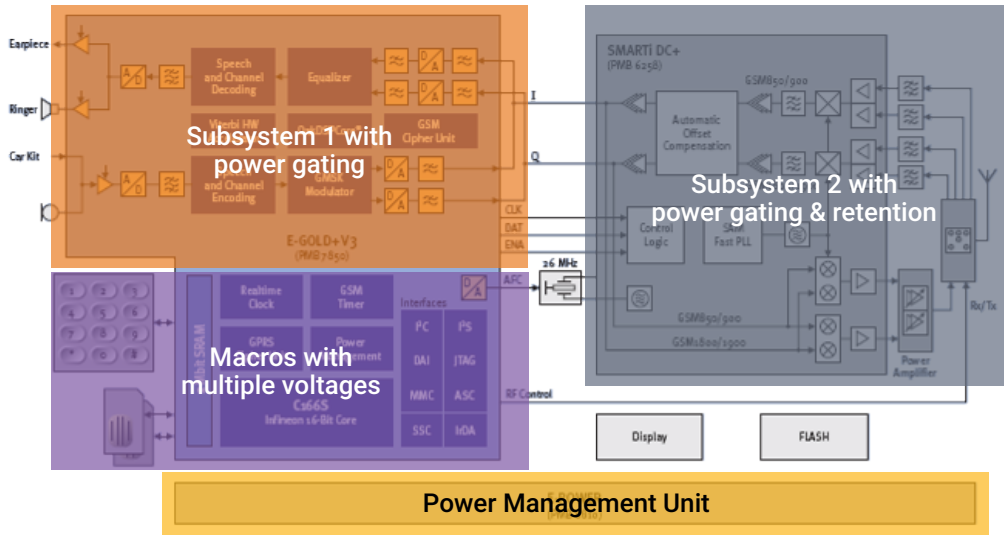


Figure 1: Power management strategy to reduce power consumption

Clock Domain Crossings (CDC) may occur at every point where a signal crosses from a source clock domain to a destination clock domain with both clock domains being asynchronous with each other (refer to figure 2). As the timing of the two clocks varies, the potential for incorrect behavior may become more prominent. Sometimes, the edges of the two clocks may align; at other times, they may vary widely.

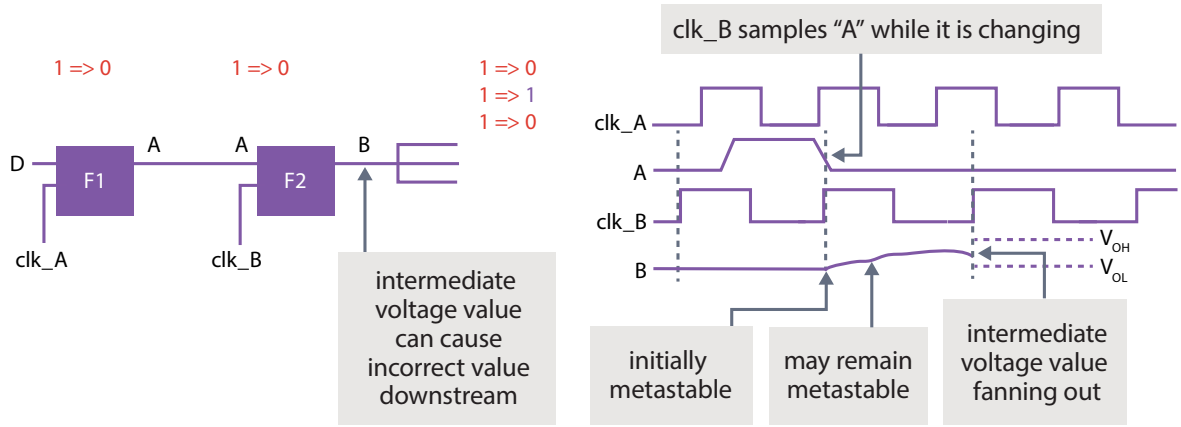


Figure 2: Metastability

The best-known consequence of CDC is metastability, a fundamental problem for designs with asynchronous clocks. If the signal from the source clock domain enters the destination clock domain and changes value closer to the destination clock edge, it may violate the setup and hold time of the resulting flip-flop, causing it to enter into a metastable state. This will cause the downstream logic to be unpredictable and put the chip in an unknown state. A common method to address such issues is adding a second flip-flop stage on the destination clock. This does not eliminate the problem, but it significantly reduces the probability that the second register will go metastable.

Low-power techniques may potentially introduce metastability especially when the power-management infrastructure interacts with signals crossing clock or reset domains. This may create additional clock-domain crossings or break the already synchronized pre-qualified paths causing silicon bug escapes typically not flagged by traditional CDC offerings. Similarly, other issues like glitches and convergence issues may be introduced due to the introduction of low-power techniques.

Isolation strategy, one of the well-known power strategies, can potentially result in the introduction of new clock domain crossings, a glitch in control, and clock path. Referring to the 1st quadrant of figure 3, after UPF instrumentation (highlighted in red), an unsynchronized path is introduced in the design between FF3 and FF2 registers in addition to pre-existing synchronous path FF1 and FF2.

Similarly, as illustrated in the 2nd quadrant, two more unsynchronized paths are added after UPF instrumentation due to save-restore pins.

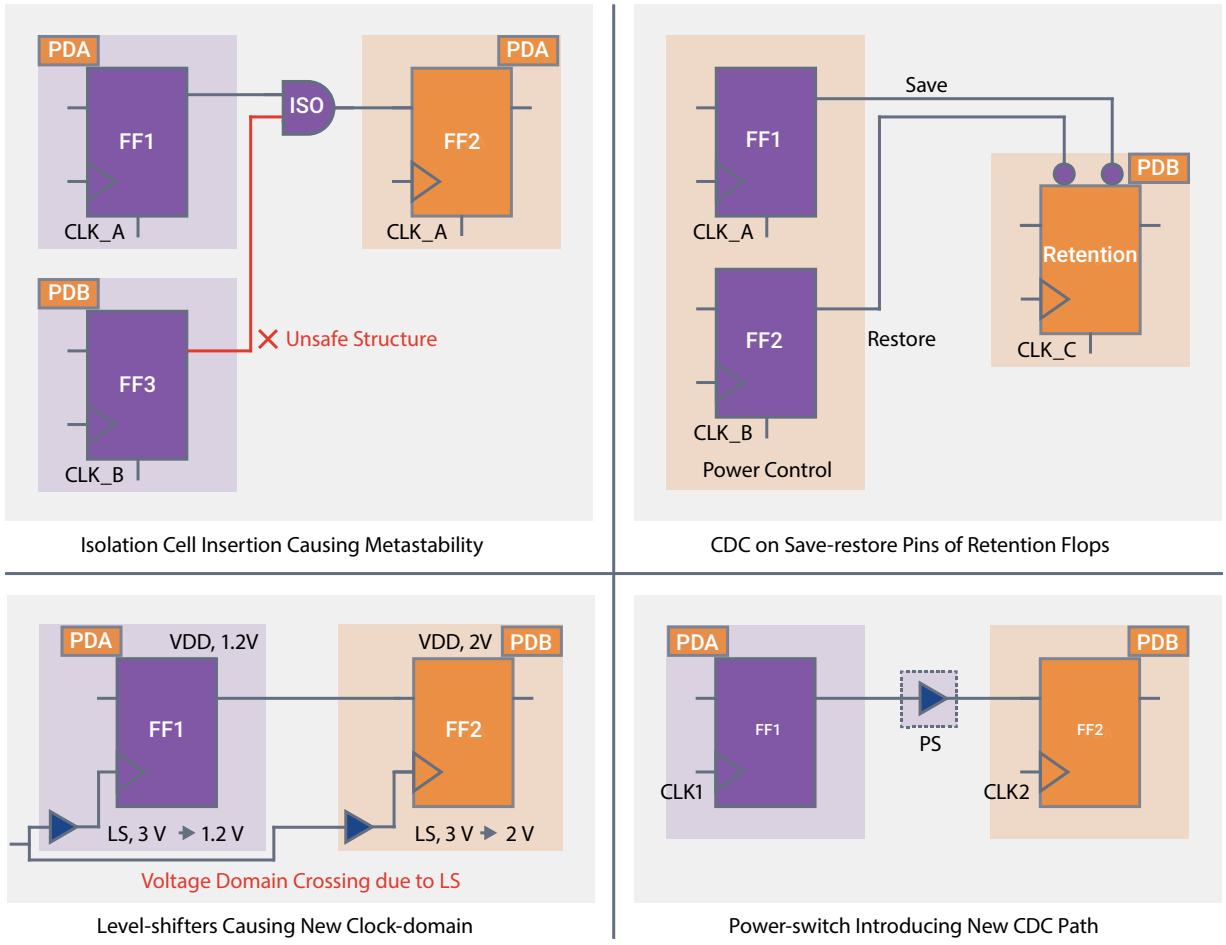


Figure 3: Design bugs introduced due to UPF instrumentation

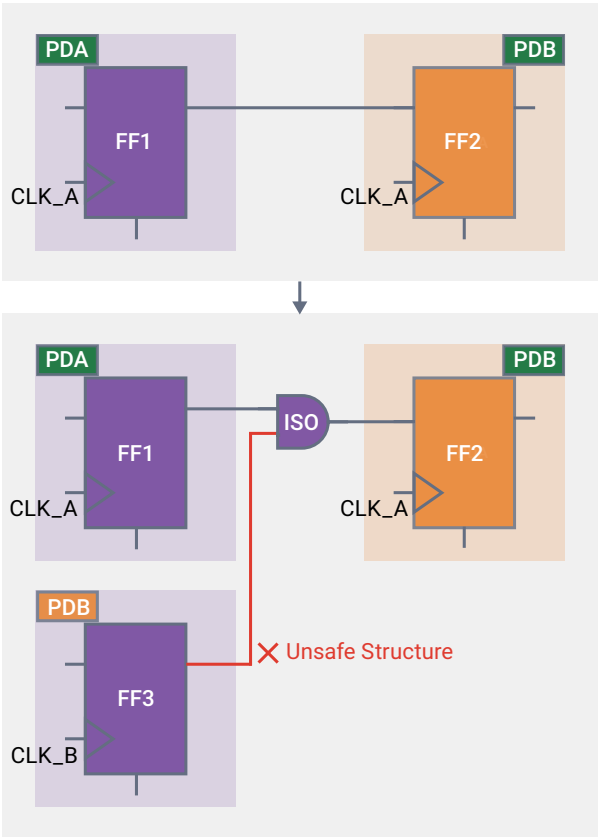
If two blocks are running on different voltages, then a level shifter is required to be specified in UPF. If these blocks interact through the synchronous path, then insertion of the level shifter on the clock path may cause CDC issues due to the different voltage domains of the clock (refer to 3rd quadrant in figure 3).

Moreover, a power switch with control and acknowledge running on asynchronous clocks can introduce unsynchronized paths in the design (refer to 4th quadrant in figure 3). Such scenarios are not visible at the RTL level but become prominent at the netlist level after UPF instrumentation.

Conventional CDC signoff offerings don't provide any mechanism for designers to check clock domain crossing issues introduced in the design due to UPF instrumentation and ensure coherency. VC SpyGlass CDC has an inbuilt UPF parser compatible with Synopsys design and verification tools that provides real instrumentation of power cells in the design and reports incremental violations caused by UPF instrumentation only.

Power Aware CDC Methodology

The power domains of the low-power design can be captured in a power intent file compatible with the IEEE Std. 1801-2015 Unified Power Format (UPF). Most of the Synopsys design and verification tools read a UPF description and create appropriate models based on the specified power intent (refer to figure 4). VC SpyGlass CDC inserts isolation cells, retention cells, power switches, level shifters, and other power structures into its internal model and factors them in during CDC analysis. All the clock domain crossing checks available for RTL signoff can be leveraged for power-aware CDC.




```
create_power_domain PDA
create_power_domain PDB

create_supply_net VDDA -domain {PDA}
create_supply_net VDDB -domain {PDB}

set_isolation ISO_EN -domain PDA -
isolation_power_net VDDB -isolation_ground_net
VSS -name_suffix ISO -clamp_value 0 -elements
{u_PDA/Q} –isolation_signal u_PDB/Q
```

Figure 4: UPF instrumentation in VC SpyGlass

The conventional CDC signoff tool either doesn't do any instrumentation or does virtual instrumentation. Virtual instrumentation may not cover all the CDC checks and flows. Hence, the signoff with virtual instrumentation at the RTL layer can lead to power issues getting detected later in the design cycle.

VC SpyGlass CDC enables real UPF instrumentation as illustrated in figure 5, ensuring upfront compatibility with Synopsys implementation tools delivering higher quality than conventional CDC signoff tools.

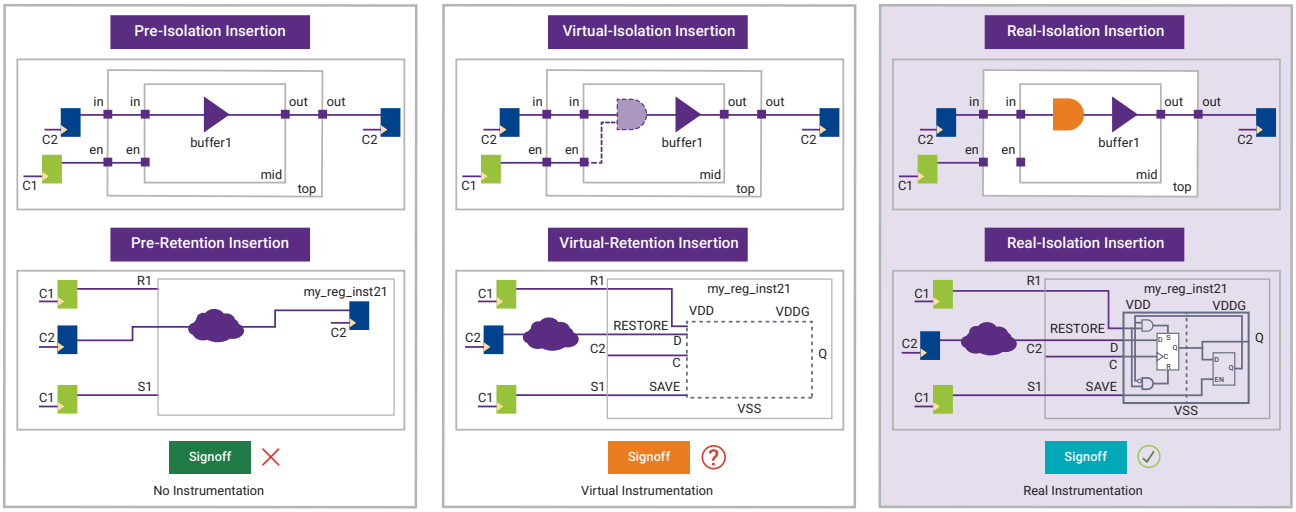


Figure 5: Real instrumentation in VC SpyGlass

VC SpyGlass CDC takes RTL, Synopsys Design Constraints (SDC), and UPF as input (refer to figure 6) and performs basic sanity checks, and further, real instrumentation is performed by inserting appropriate power cells in the design. Once the internal design model is ready with inserted UPF cells for CDC verification, all the RTL checks can be applied to UPF instrumented design.

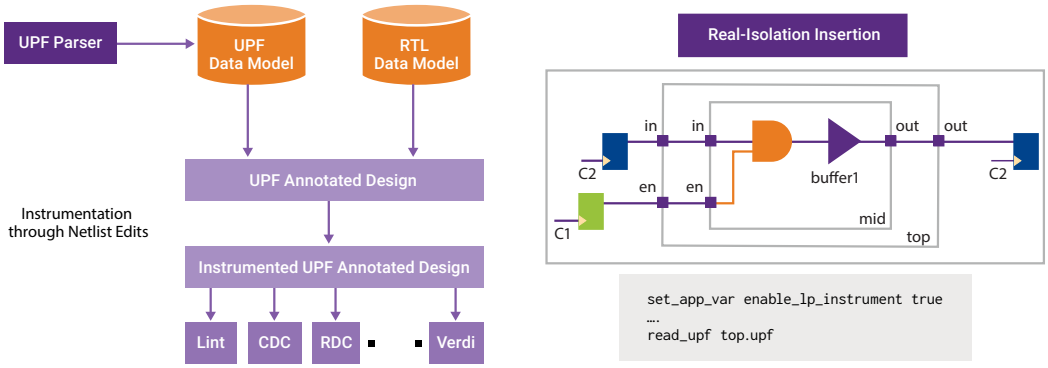


Figure 6: VC SpyGlass UPF-aware methodology

VC SpyGlass performs all the RTL level checks to identify missing synchronizers, glitches, and convergence problems in the design. It reports all the incremental violations due to UPF instrumented cells in the design with a specific reason code. Designers can simply identify the differences between pre-UPF and post-UPF designs using the inbuilt compare_violation feature (refer to figure 7).

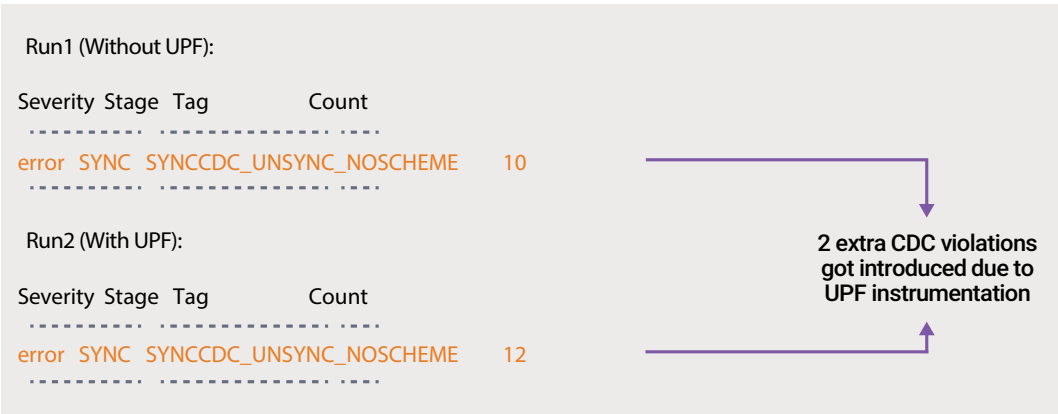


Figure 7: VC SpyGlass compare_violations feature results

Native integration with Synopsys Verdi debug helps to quickly identify power cells residing on clock domain crossing paths for faster debug. The designer can easily cross-probe instrumented power cells within Verdi. Furthermore, the designer can get deeper insights into power cell properties when clicking on UPF instrumented cell in Verdi schematic (refer to figure 8).

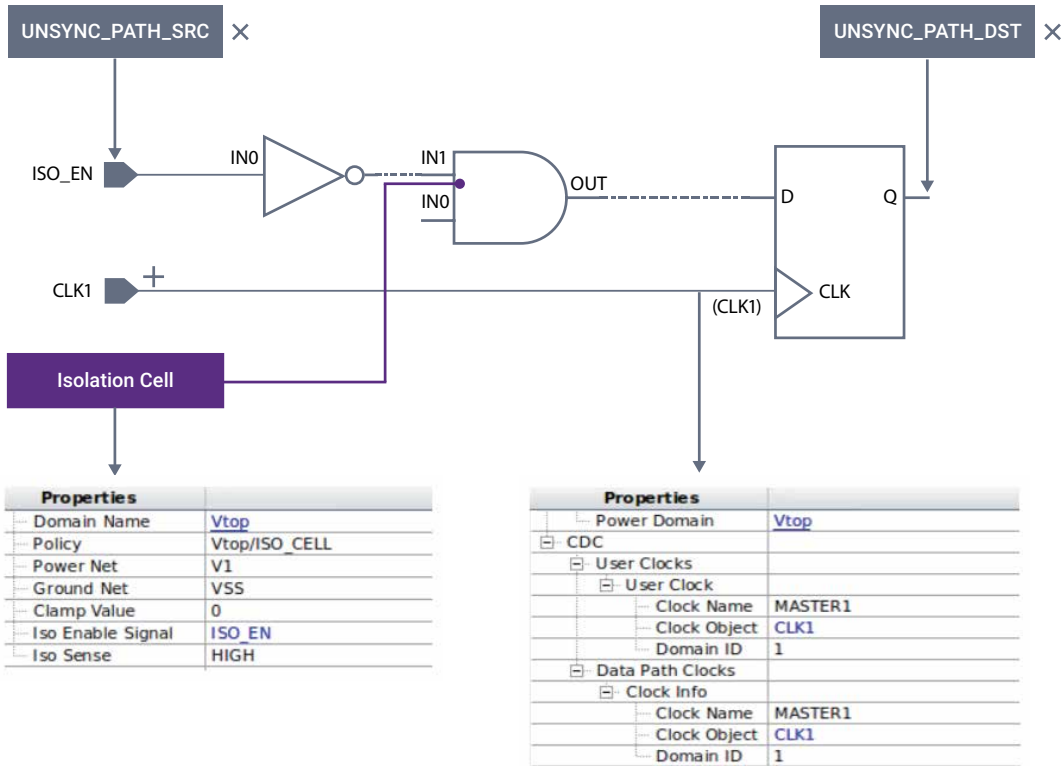


Figure 8: Unsynchronized crossing due to UPF instrumentation

A powerful TCL interface is also available for querying power cells and applying constraints. For example, clock domain crossing with power domain crossing can be identified using the below TCL command.

```
vc_static_shell> get_cdc_paths -from clk1* -to clk2* -filter “power_domain_crossing==true”
```

Conclusion

SoC design sizes in modern chip design continue to grow resulting in the increased use of low power techniques to reduce power consumption. The introduction of these power cells late in the design cycle raises concerns such as breaking pre-qualified paths, metastability, glitch and convergence resulting in chip-killing bugs.

Synopsys VC SpyGlass CDC power-aware methodology addresses all these concerns. VC SpyGlass provides an unrivaled solution for determining all types of CDC issues originating due to new low-power logic introduction at the RTL stage. This methodology ensures consistent UPF support and intuitive debugging, ultimately enabling complete static signoff for low-power designs.

06/23/22.CS900574795-VC-SpyGlass-Power-Aware-WP.

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