

# Achieving CDC Signoff on Multi Billion Gate Designs with Hierarchical CDC Flow

## Author

**Navneet Chaurasia**  
Sr Applications Engineer,  
Synopsys

## Overview

For the last few decades, the System-on-Chip (SoC) design size has dramatically increased and more complexity has been introduced to deliver the desired functionality. A typical SoC can have many complex IPs operating at different clock frequencies, which can stress the verification cycle. Generally, design and verification teams are spending an increasing amount of time to ensure that the SoC matches its design specification.

The verification cycle can be reduced drastically by ensuring functionality of IPs that can be achieved by verification at the IP level. Once IPs are qualified as per design specifications, then SoC logic and IPs interfaces can be verified to ensure that there is no metastability, convergence, coherency etc.

Synopsys next-generation VC SpyGlass™ RTL signoff platform has the capability to extract IP level interface information that can be plugged-in at the SoC level to verify inter-block crossings, convergence and glitch prune logic to meet design specifications.

This white paper talks about VC SpyGlass' hierarchical CDC signoff methodology to verify clock domain crossing problems at the SoC level.

## Challenges in CDC Signoff on Multi Billion Gate Designs

Design complexity has increased due to higher speed and low power consumption requirements. For increased speed, more complex clock logic is introduced to operate chip at higher frequency and in order to save power, some portions of the SoC are turned off when inactive.

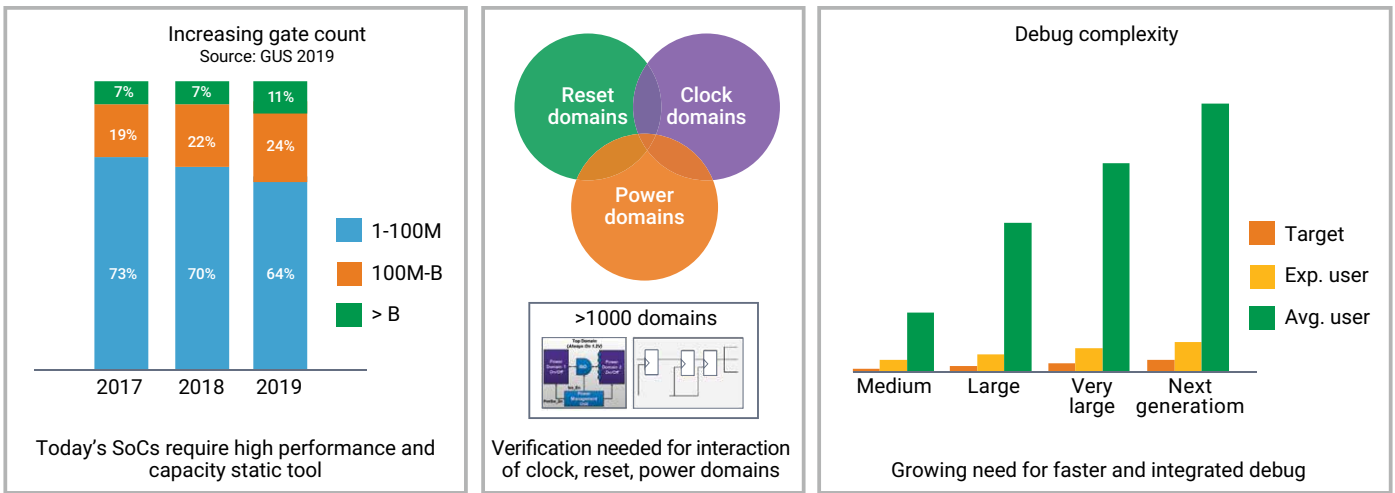


Figure 1: Gate count vs design complexity and challenges

Increased gate count and asynchronous clock domains (shown in figure 1) at the SoC-level stress the verification cycle by flagging millions of metastability, convergence, coherency and glitchy problems that must be fixed to achieve design specifications.

A CDC occurs at every point where a signal crosses from a source to a destination clock domain and they are asynchronous to each other. As the timing of the two clocks varies, the potential for incorrect behavior can become more prominent. Sometimes the edges of the two clocks may align; at other times they may vary widely.

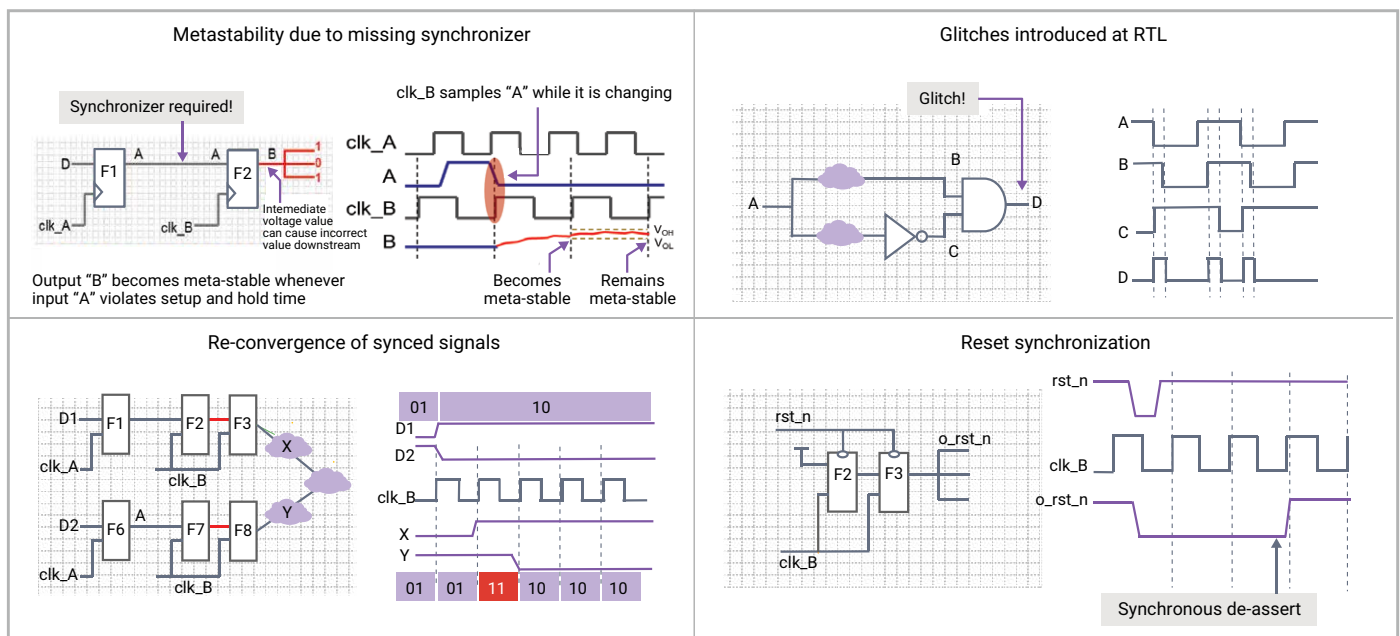


Figure 2: Metastability, convergence, glitch and reset synchronization

The fundamental consequence of CDC is metastability, a well-known problem for designs with asynchronous clocks. If the signal from the source clock domain enters the destination clock domain and changes value close to the destination clock edge then it may violate the setup and therefore the hold time resulting flip-flop capturing the signal may go into a metastable state, which will drive the downstream logic and put the chip in unknown state. A common method to address such issues is adding a second flip-flop stage on the destination clock. This does not eliminate the problem entirely, but it reduces the chance that the second register will go metastable to a very low probability.

Similarly, if two signals from the source domain are synchronized independently (shown in figure 2) and then converge in the destination domain, they can be offset by one cycle and incorrect results will be generated. Divergence occurs when a single signal in the source domain is synchronized twice and used in two different areas of the destination domain where the synchronized values must be identical. Again, because of clock variation and metastability, the two synchronizers of the same source signal may produce destination signals offset by a cycle.

Signal glitches in synchronous paths are momentary and harmless (see Figure 2) and don't violate setup and hold requirements. But across a CDC, glitches may be interpreted as valid value changes if they happen to be clocked into the destination domain.

## Hierarchical CDC Signoff Methodology

Synopsys' VC SpyGlass platform addresses these challenges very easily with multi-core support and advanced techniques to reduce noise. It is natively integrated with Synopsys Verdi® automated debug system to accelerate root cause analysis for bugs. It also uses design setup and Tcl commands consistent with Synopsys Design Compiler® and PrimeTime® tools to significantly reduce setup time between implementation and verification flows.

With rapidly growing designs sizes, performing CDC analysis in a single run at the SoC level is challenging because of performance/capacity, report volumes, and alignment with design cycle issues. Design development cycles usually follow the bottom-up approach. Hierarchical CDC approach is best suited for such development cycle. The approach is efficient in managing CDC reports because design blocks are locally signed-off and the SoC integration team reviews the CDC-issues coming at SoC-level only.

The hierarchical flow in VC SpyGlass platform (shown in figure 3) is based on the design abstraction approach to generate accurate top-level CDC reports, which is similar to the reports generated in a flat run but excludes the IP level reports, making them easy to comprehend and manageable. Design abstraction retains the relevant block level logic (shown in figure 4) called signoff abstract model (SAM), which is needed to perform SoC level analysis to achieve 100% accuracy. This approach gives all the crossings, convergence and glitch problems except the violations that are completely lying inside blocks whose SAM models are provided. Using this methodology, IP and SoC designers have to analyze the violations coming inside IP and SoC respectively which reduces the verification cycle and improves the productivity.

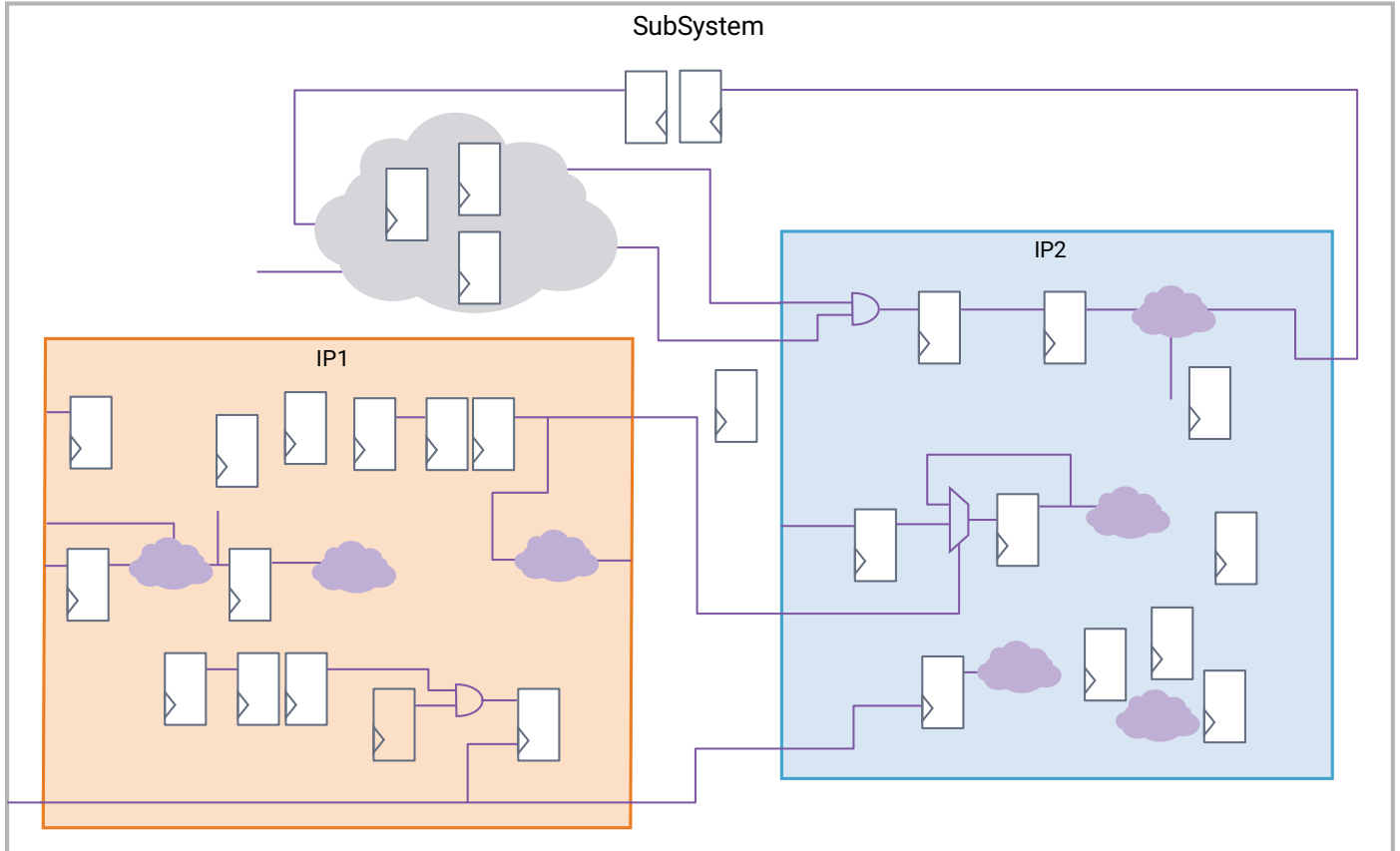


Figure 3: Flat design view (including IP1 and IP2 logic)

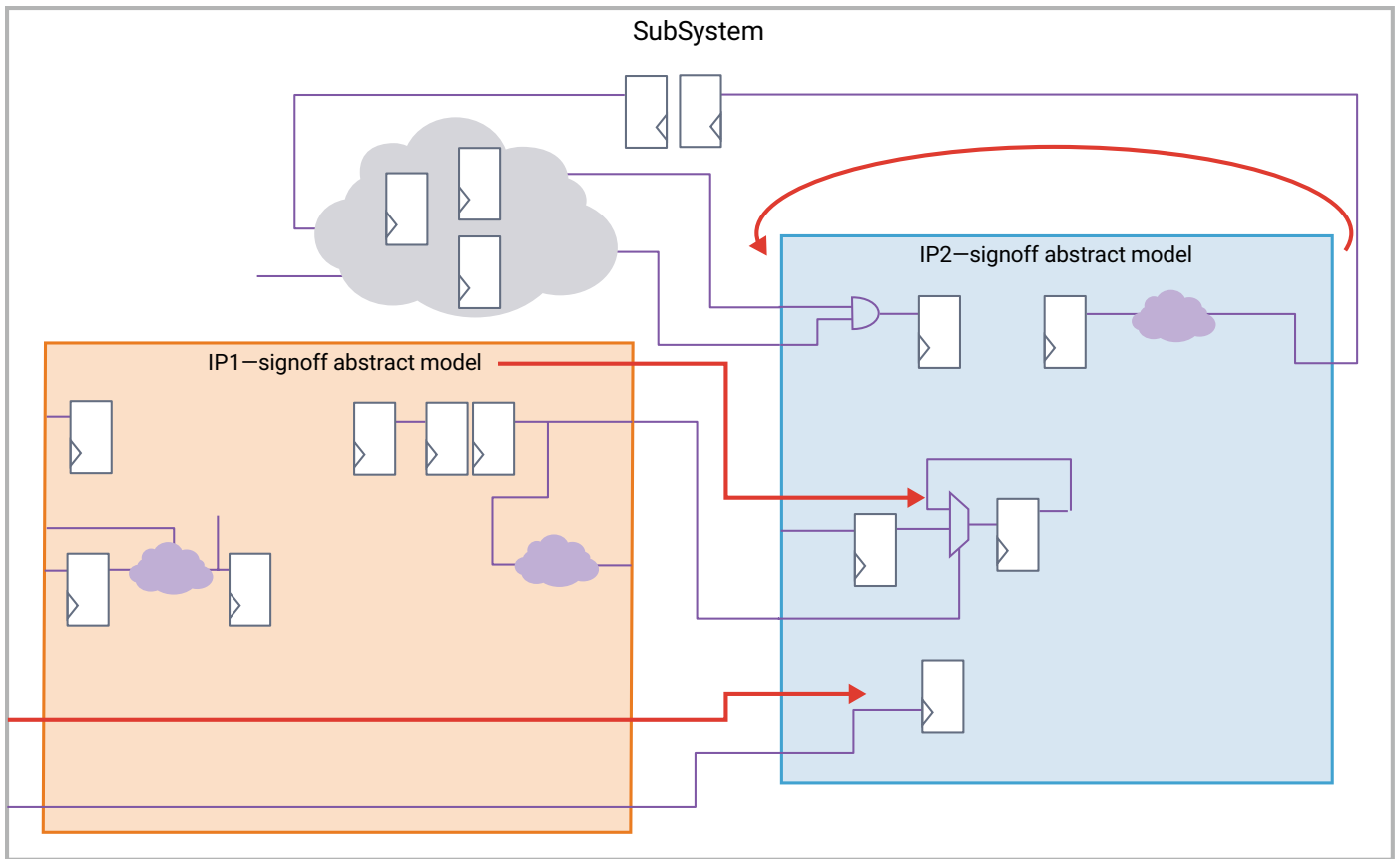


Figure 4: Flat design view (including IP1 and IP2 abstracted model)

Designers can qualify the IPs by fixing all the clock domain crossing issues at IP level and then generate the signoff abstract model to extract interface information. The interface information is then plugged-in at the chip level to verify the IPs interfaces. Once the signoff abstract model gets imported at chip level then next step is to validate block assumptions like clock, reset, constant and quasi static etc., to find out mismatches between block level assumptions and actual constraints propagation from chip level.

The signoff abstract model extracts the boundary logic which plays a vital role in clock domain crossings, convergence, coherency and glitch at chip the level. This technology provides a great advantage to the SoC integration team, enabling them to see the IP-level logic and possible CDC issues, which helps them to guide the IP team to uncover actual root cause and resolve.

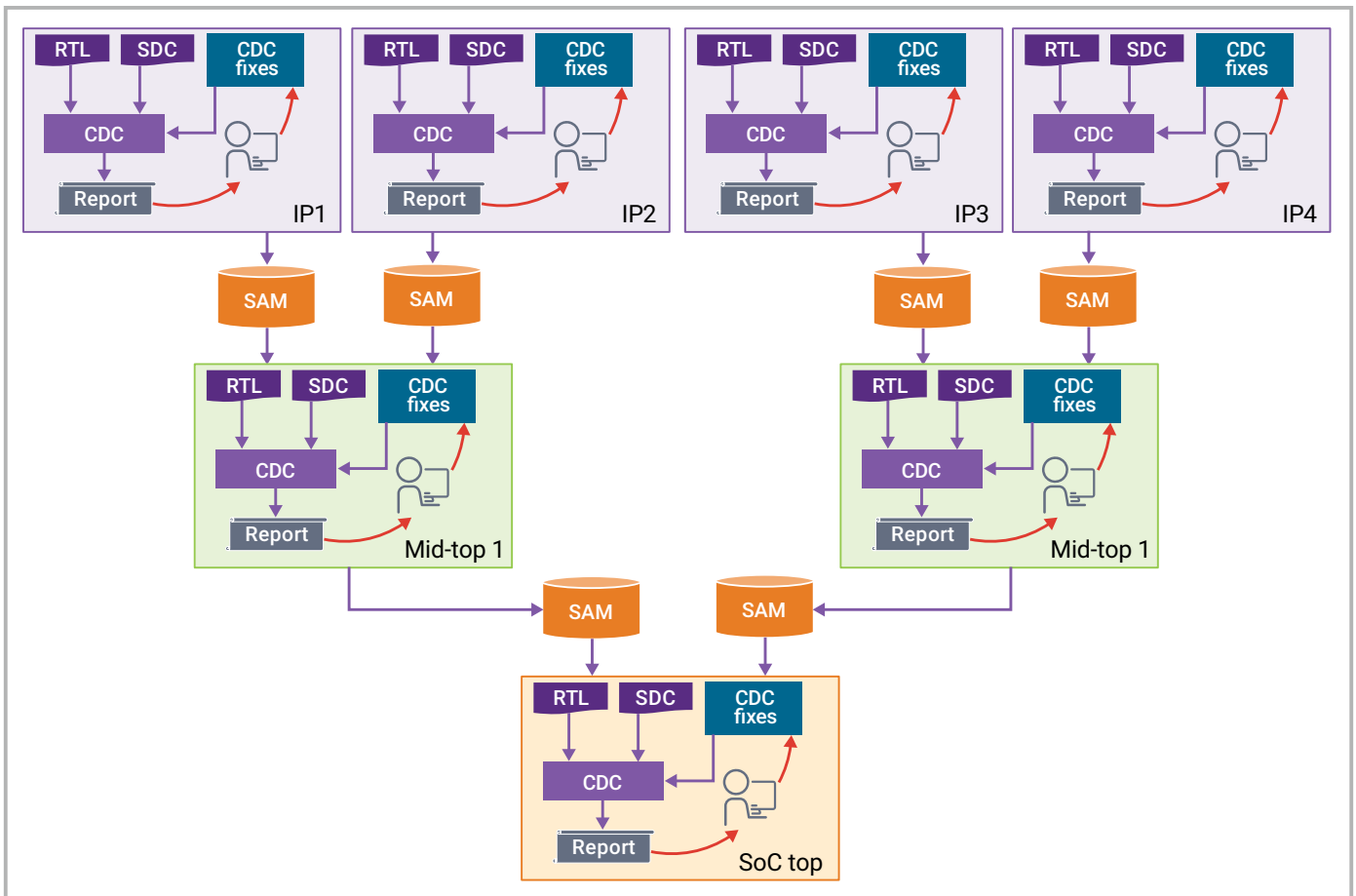


Figure 5: Bottom-up CDC signoff methodology

In the bottom-up CDC signoff methodology (shown in figure 5), once the IP1, IP2, IP3 and IP4 are qualified then signoff abstract model for the same is generated to abstract the IP level interface information. These models need to be plugged-in at “Mid-Top1” and “Mid-Top2” for the subsystem-level CDC verification.

After qualification of “Mid-Top1” and “Mid-Top2” the signoff abstract model is generated for both the subsystem-level runs for reuse at chip level for CDC verification.

The SAM-based hierarchical flow offers the following advantages:-

- The top-level CDC run reports generated with VC SpyGlass CDC are the same as flat run reports without the block-level reports
- Block SAMs are loaded as part of design elaboration at the top-level runs and remaining flow is the same as flat run. Therefore, SAM-based hierarchical flow is more stable and less error prone
- Waivers created in the SAM-based flow, which retains CDC relevant objects, can be transformed to apply to flat run, if needed
- Encrypted modules are automatically supported and do not require any special handling in the SAM-based hierarchical flow
- This approach has 100% coverage with CDC checks including sequential convergences

## Conclusion

Along with many other metrics, the number of clock domains in modern chip designs has been growing rapidly and will continue to grow for the foreseeable future. In modern SoCs, most of the IPs are obtained from third-party vendors where semiconductor industries don't share the RTLs due to their internal protocols. The methodology described in this whitepaper helps IP designers to generate an encrypted abstract model at IP level, which can be reused identically, at SoC level for the CDC verification.