SYNOPSYS®
Predictable Success

Accelerating Analog Simulation with HSPICE Precision Parallel Technology

September 2010

Authors

Robert Daniels
Sr. Staff Engineer,
Synopsys Inc.

Harald Von Sosen
Principal Engineer,
Synopsys Inc.

Hany Elhak
Product Marketing Manager,
Synopsys Inc.

Executive Summary

Modern mixed-signal IC designers must cope with the requirements of complying with the latest high-speed communication standards, advanced process node effects and extended battery life while meeting aggressive project schedules. Such requirements offer serious challenges to the accurate simulation of analog and mixed-signal designs. For example, analog designers employ digital control to configure analog blocks for multi-standard systems and to calibrate for process variations in advanced nodes. Such techniques significantly increase circuit simulation run times at a given process, voltage and temperature (PVT) corner. Furthermore, additional PVT-corner simulations are needed for advanced process nodes. As a result, analog design teams need to run longer simulations, and run more of them, while maintaining silicon-accurate results.

An effective way to address this challenge is to use SPICE algorithms to take full advantage of the latest multicore processor hardware. The new Precision Parallel (HPP) technology in Synopsys' HSPICE® circuit simulation tool delivers highly-scalable performance on today's multicore computers with up to 7X simulation speed-up for analog and mixed-signal designs. Using HPP, design teams can accelerate verification of their analog circuits across process variation corners, meet their project timelines and reduce the risk of silicon respins.

Introduction

HSPICE Precision Parallel technology is a new multicore transient simulation extension to HSPICE for both pre- and post-layout of complex analog circuits such as PLLs, ADCs, DACs, SERDES, and other full mixed-signal circuits. HPP addresses the traditional bottleneck in accelerating SPICE on multicore CPUs with new algorithms that enable a larger percentage of the simulation to be parallelized, with no compromise in golden HSPICE accuracy. Additionally, efficient memory management allows simulation of post-layout circuits larger than 10 million elements.

Challenges in Accelerating SPICE

A typical SPICE simulation analyzes the circuit on a large number of time steps. Each time step consists of multiple iterations, each of which can be broken down into two major tasks:

- Evaluating the devices in the circuit and loading them into a matrix
- Solving the matrix to calculate voltage and current at each node

The iterations continue until the circuit converges, then the simulator moves to the next time step and repeats the same process.

The percentage of simulation time spent in evaluating the devices and solving the matrix is dependent on circuit type. The key to accelerating SPICE on a multicore CPU is to be able to parallelize as much of each individual task as possible without sacrificing accuracy.

Device evaluation is the dominant activity for small pre-layout circuits. This may take up to 75% of the simulation time and scales linearly with circuit size. Traditional SPICE simulators distribute this task on multiple CPUs, achieving a modest level of parallelization. Leaving more than a third of the simulation in sequential tasks, one can only expect 2-3X speedup using 8-core machines, as Amdahl's law predicts. Figure 1 depicts how performance plateaus when multi-threading a hypothetical circuit on 2-, 4- and 8-core machines.

Scalability is even worse on large post-layout circuits where device evaluation represents less than half the simulation time. Solving the matrix can consume more than 50% of the simulation time for large post-layout circuits. Significant scaling can be achieved by parallelizing this task, however, solving a sparse matrix (the typical matrix form for electronic circuits), involves a great deal of sequential activities. Traditional SPICE simulators scale poorly. Even with 90% efficiency, Amdahl's law predicts a theoretical speedup of 5X on 8 cores, as shown in Figure 1. The scaling is further limited by the speed of data as it moves between processors and memory. The actual speed-up can be less than 3X on 8 cores.

To obtain highly-scalable computations, the parallel efficiency of the underlying code must be very close to 100%, as shown in Figure 1. Another simulation challenge is that the order of data processing is not cache-efficient. Cache efficiency is important for multicore performance because processors compete for cache and memory access.

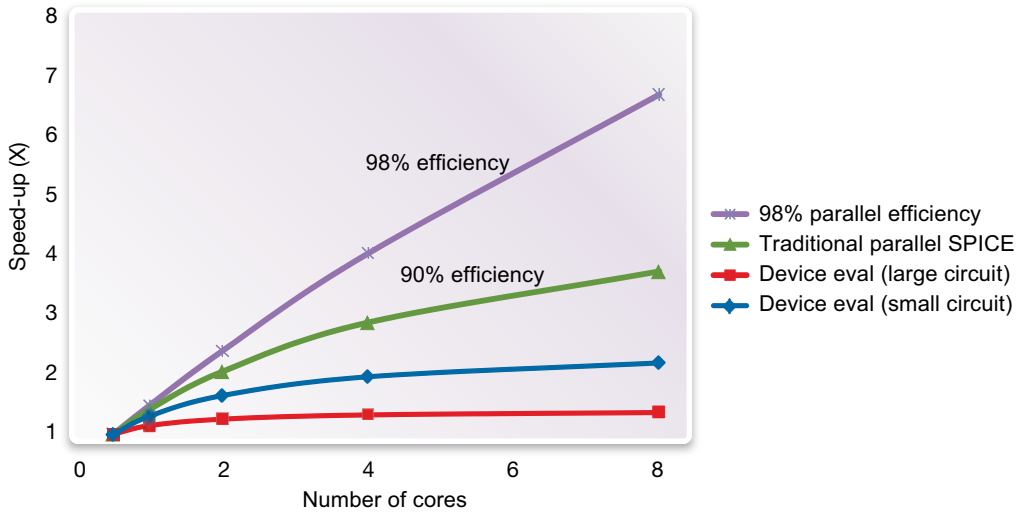

Figure 1: Theoretical limits of parallel SPICE simulation (Amdahl's Law)

HSPICE Precision Parallel Technology

HPP applies several new algorithms to the transient analysis problem. This includes improving single-thread computation, implementing a highly-scalable approach to take full advantage of multicore machines, and, finally, optimizing the memory management with a compact memory footprint and efficient cache utilization. These improvements have been implemented in HPP while maintaining full accuracy.

Single-Core Speed

Modern analog circuits consist of components that operate at different time constants. For example, a PLL consists of a voltage-controlled oscillator and divider operating at a high frequency, while other circuit components such as the phase detector, filter and digital control circuitry operate at much lower speed. The adaptive sub-matrix algorithm in HPP technology manipulates the matrix in such a way that slower parts of the circuit can be solved in fewer iterations than the faster ones, significantly improving the overall simulation speed. Figure 2 shows the average HSPICE speed improvements over the past three years. The HPP technology in the 2010.12 release delivers an average 40% speed-up over the previous release.

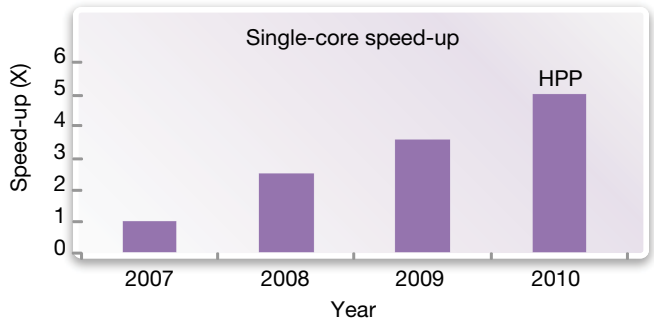

Figure 2: Single-core speed improvement in HSPICE

Multicore Scaling

HPP technology uses an adaptive sub-matrix algorithm--a highly scalable algorithm that divides the matrix solving stage into smaller tasks that can be efficiently performed on multiple CPU cores. In addition, it parallelizes other small tasks such as output and time step control to achieve parallelization efficiency close to 100%. The result is up to 7X scaling on 8 cores, a significant improvement over the previous release. Figure 3 shows HSPICE multicore scaling on representative analog/mixed-signal circuits such as Sigma-Delta data converters and PLLs.

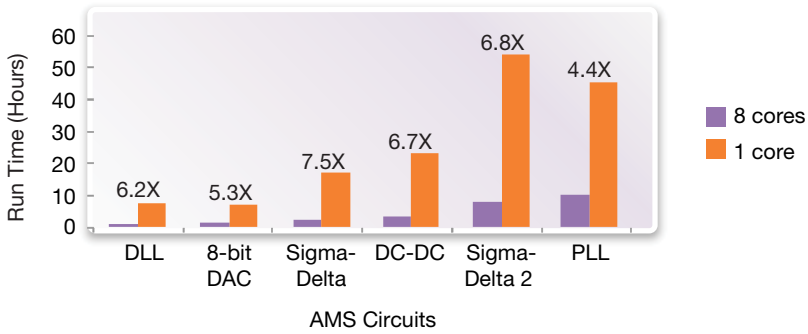

Figure 3: HSPICE multicore scaling on representative analog/mixed-signal circuits

Cache Efficiency and Memory Bus

Even with almost 100% parallelized code, the actual scaling achieved will be limited by cache misses and the finite time required in moving data between cache and main memory. The degree to which cache misses and data movement affect the overall scaling depends on the machine parameters, e.g., cache size, memory bus speed and the efficiency of the code (e.g., localization and minimization of data). HSPICE uses very efficient localization of data in blocks that are comparable in size to the highest-level cache. The variable controlled by the user is the multicore architecture on which HPP is run. Generally, the larger the cache (second- or third-level) and the faster the memory bus, the better performance and scaling.

The attention to memory efficiency also provides the benefit of high capacity. HPP is capable of simulating post-layout circuits in excess of 10M elements and 9M nodes. Figure 4 demonstrates HSPICE capacity improvements over the past three years. The HPP technology contributes 25% capacity improvement on average over the previous release.

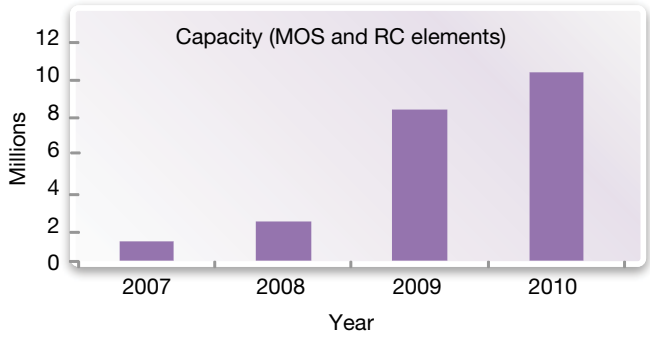

Figure 4: HSPICE capacity improvement from 2007 to 2010

Conclusion

HSPICE Precision Parallel technology is a new multicore transient simulation extension to HSPICE for both pre- and post-layout circuits, including PLLs, ADCs, DACs, SERDES, and other full mixed-signal circuits. HPP achieves higher performance on multicore machines by removing a bottleneck that had slowed down multi-threaded simulations in the past. It efficiently utilizes the scalability available from today's multicore architectures, with the best performance coming from machines with the largest second-/third-level cache and fastest memory bus. Efficient memory management allows simulation of post-layout circuits larger than 10 million elements. In addition to the new HPP technology, the HSPICE 2010 solution includes enhanced convergence algorithms, advanced analog analysis features and foundry-qualified support for process design kits (PDKs) that extend HSPICE gold-standard accuracy to the verification of complex analog and mixed-signal circuits. With HSPICE 2010, design teams can accelerate verification of their analog circuits across process variation corners, and minimize the risk of missing project timelines and silicon respins.

SYNOPSYS®
Predictable Success
Synopsys, Inc. • 700 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com