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CustomExplorer Ultra

Automated Regression for Mixed-Signal Verification

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Introduction

CustomExplorer™ Ultra represents the next generation in mixed-signal verification environment, including regression management, debug and analysis for complex SoC design. Modern mixed-signal SoCs have highly intermixed analog and digital content, requiring advanced strategies to deal with the many issues involved in achieving high verification productivity. CustomExplorer Ultra meets these challenges by providing an advanced regression and analysis environment for mixed-signal verification, including automated regression setup and job control, at-a-glance pass/fail visualization, advanced post-simulation analysis, and debug. CustomExplorer Ultra is also seamlessly integrated with both CustomSim™ and CustomSim/VCS®, creating a complete solution for mixed-signal verification.

Mixed-signal Verification Challenges

As SoC designs increase in complexity and analog content continues to grow, mixed-signal teams face an ever-increasing challenge in achieving high-quality verification, while also improving verification productivity.

For complex mixed-signal SoCs, hundreds or thousands of corners may need to be simulated, resulting in the need to set up and track a multitude of simulation runs while wading through numerous large simulation log files and output files. Once the simulation jobs are completed, design teams need to analyze the results and decide which runs are successful, which runs need further debug and analysis, and then repeat this process until they reach their verification goals.

Additionally, IP blocks can come from many different sources, including different schematic environments or standalone netlists. These blocks also have multiple views containing a mix of languages, such as SPICE, Verilog, Verilog-A, Verilog-AMS, and SystemVerilog. Depending on the level of required accuracy and the type of circuit, design teams may need to run various configurations of a block and use different simulators such as HSPICE®, CustomSim, or CustomSim/VCS.

As the level of verification increases, from circuit-level to block-level to chip-level, the complexity of the verification problem also increases. Many full-chip simulations must be run in parallel and with different levels of modeling (transistor-level, Verilog-A, Verilog, etc.) as the verification focus shifts to different parts of the circuit. To manage the different levels of modeling, testbench and netlist configurations must be switched as quickly as possible between the numerous simulation runs (see Figure 1). Fast test turnaround time (TAT) is a critical element of maintaining high levels of verification productivity, assuming accuracy and capacity needs are met.

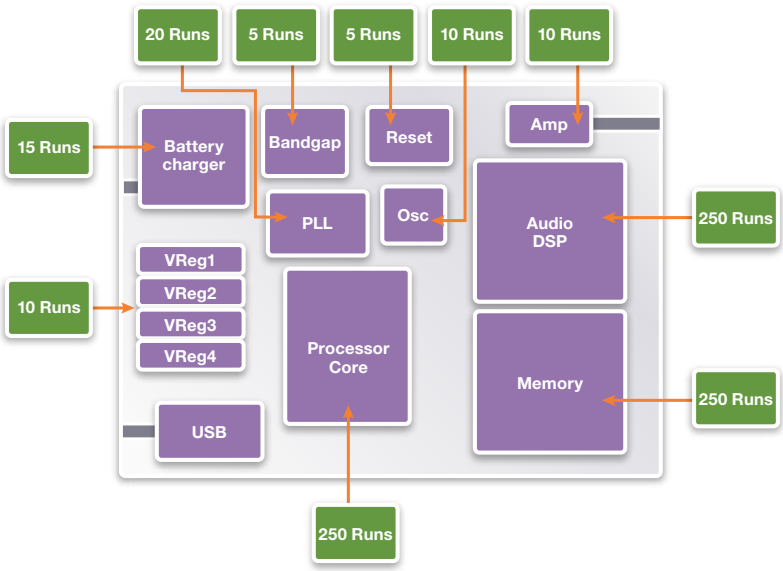

Figure 1: Top-Level Verification Simulation Takes Many Corners and Configurations

A common, but inadequate, solution for mixed-signal verification is to try and manage regressions directly out of a schematic environment. Another common solution is to try and use a scripting language, such as tcl, Perl, or Python, in a command-line environment.

Schematic environments are optimized for an interactive design process, and they don't scale to large SoC verification applications. For instance, all of the various IP blocks must be in the schematic environment, making it difficult to support heterogeneous netlists (i.e., netlists from multiple sources or environments). Each test configuration must be separately netlisted out of the schematic environment, which can be very time-consuming and prone to errors (see Figure 2). Also any schematic changes require re-netlisting, or at least managing incremental netlists. Finally, large design groups may find it difficult to ensure that others are not editing the schematic database and locking it. Locking can be an issue when multiple configurations need to be netlisted out of the schematic database. If a cell in the design hierarchy is opened by another user, that cell is locked and can't be modified by the verification engineer trying to change the schematic to create the correct configuration for netlisting. Since schematics databases are meant to be used concurrently by multiple members of a design team, this is a difficult problem to manage. A netlist-driven solution can avoid this problem by using simple file system write permissions, as no concurrency is needed.

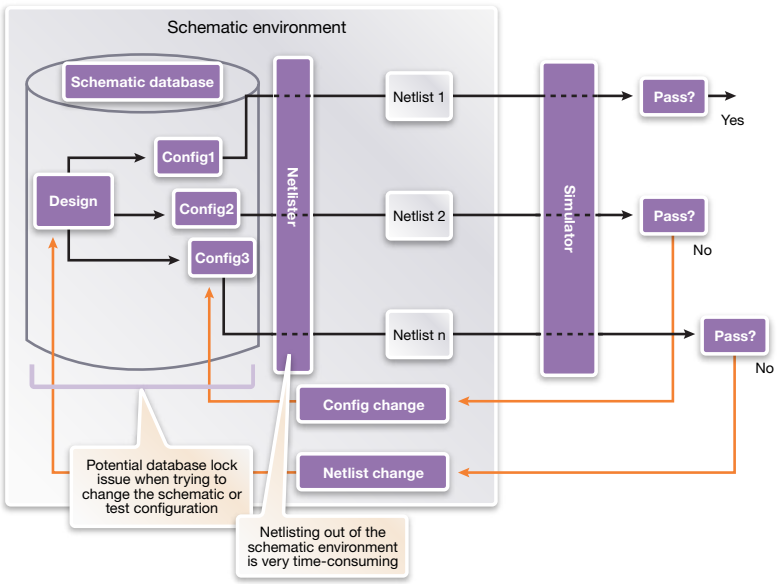

Figure 2: Schematic-based Flow and Issues

Using script-based verification developed in-house also has its challenges. Script-based approaches can potentially alleviate some of the issues outlined above in that they can handle heterogeneous netlists and changes don't require re-netlisting (see Figure 3). But scripts are usually created ad-hoc without considering reuse and are not easily customizable by other users. Common reuse issues in custom scripts include hard-coded paths, lack of setup-save-and-recall, and no common or managed project area for scripts. It can also be difficult to collect all of the elements of the regression for reuse, such as which blocks are associated with which test configuration. Scripts must also be maintained to adapt to new requirements, which can be a problem if they are not well-documented. Finally, home-grown, script-based verification lacks a sophisticated analysis and debug environment to accelerate results viewing, analysis and debug. Solutions developed in-house become difficult and expensive to maintain in the long run.

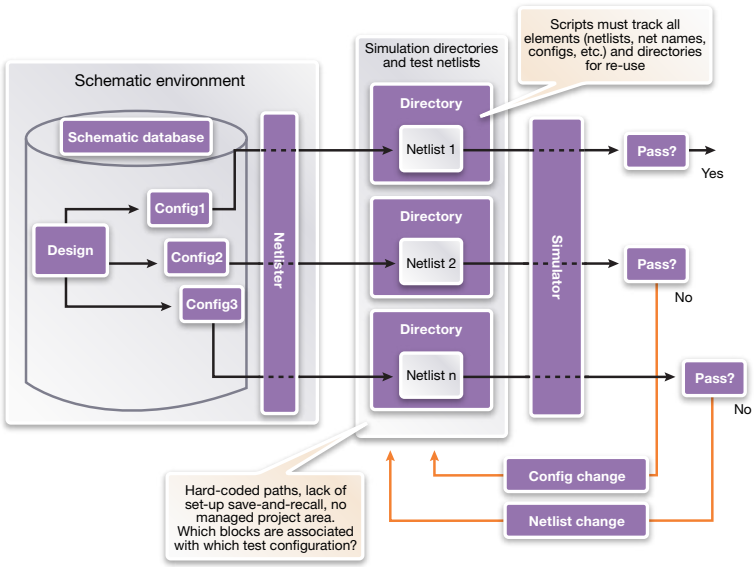

Figure 3: Script-based Flow and Issues

CustomExplorer Ultra Solution

To advance the state-of-the art in mixed-signal verification, Synopsys developed CustomExplorer Ultra, a netlist-based verification regression management, debug and analysis environment for complex mixed-signal SoC designs. Combined with CustomSim and the CustomSim/VCS mixed-signal simulation solution, CustomExplorer Ultra provides a scalable environment for mixed-signal SoC verification.

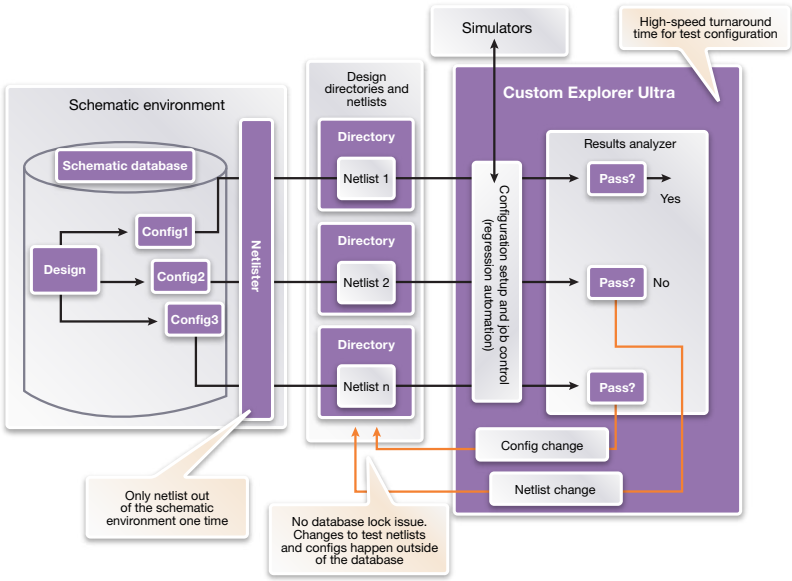

Figure 4: CustomExplorer Ultra

Heterogeneous Netlists Assembly

CustomExplorer Ultra can import many different formats of netlists (i.e., heterogeneous netlists) which can be from almost any environment or netlist source. These netlists can contain a wide variety of mixed-signal content, including SPICE, Verilog, Verilog-A, Verilog-AMS, and SystemVerilog. These imported netlists can then be configured and assembled into a single netlist that is targeted to a specific simulator. For example, you can configure blocks with a mixture of SPICE and Verilog models and use CustomSim/VCS for mixed-signal simulation. Or configure a block as only using SPICE models and target CustomSim for all transistor-level simulation.

Regression netlists can be quickly and easily retargeted at any time to a different simulator. CustomExplorer Ultra's ability to quickly assemble heterogeneous netlists with multiple types of mixed-signal content allows design and verification teams to effortlessly create a higher-level SoC netlist and prepare the design for regression testing that will scale to larger mixed-signal SoC design sizes.

Regression Automation

CustomExplorer Ultra provides an easy-to-use environment for setting up multiple testbenches and simulation corners. After setup, simulation jobs are automatically generated, queued, and submitted to the CustomSim or CustomSim/VCS server cluster. A simulation regression job distribution and monitoring panel provides real-time status of all jobs running on multiple machines, providing quick feedback if problems are detected during simulation.

CustomExplorer Ultras' simulation job generation saves significant time, as complete simulation jobs for the target simulator are automatically created for each test configuration. Any test configuration parameter (including the target simulator) can be easily changed at any time via the Test Configuration menus, and a complete set of regression simulation jobs will be automatically regenerated. This auto-generation capability is much faster than generating simulation decks from a schematic environment and is easier to reuse than a custom script.

Advanced Analysis

Simulation results are post-processed and presented in a spreadsheet-style Results Analyzer window, providing a visual summary of the verification tests with at-a-glance pass/fail visualization. These test results can also be filtered by design, design variables, equation results, or equation expressions. The unique, programmable Waveform Compare technology in CustomExplorer Ultra can be used to compare simulation results to a known-good waveform, saving considerable analysis time. An example of advanced debug with CustomExplorer Ultra's Waveform Compare is to compare a pure Verilog simulation waveform file (like vcd) to a transistor-level FastSPICE simulation waveform file (like wsf). In addition to comparing the FastSPICE simulation results for errors in the logic states compared to the Verilog simulation, Waveform Compare can detect other types of errors, such as glitches, overshoot, undershoot, or slow rising or falling edges.

Debug

The CustomExplorer Ultra debug environment provides comprehensive SPICE linting utilities, design hierarchy file browsing and signal tracing, as well as cross-probing between netlists and an auto-generated connection visualization for rapid debugging. CustomExplorer Ultra includes Custom WaveView™, enabling waveform cross-probing and sophisticated waveform measurements with equation-based post-processing, as well as built-in advanced analysis features such as eye diagrams and ADC measurements (DC static characteristics, AC dynamic characteristics, jitter, etc.). Equations can be modified at any time and results displayed without running the simulation again. Signals can be fully traced across analog and digital boundaries, from a transistor to a gate. Together, these features aid designers in rapidly performing customized advanced analyses in a powerful mixed-signal design debugging environment.

Conclusion

CustomExplorer Ultra is the latest verification environment for managing complex mixed-signal verification regressions and performing advanced analysis of analog and mixed-signal designs. CustomExplorer Ultra's advanced set of regression and analysis features can dramatically improve mixed-signal verification productivity and is scalable to large, complex mixed-signal SoCs. When combined with Synopsys' CustomSim and CustomSim/VCS mixed-signal simulation solutions, CustomExplorer Ultra provides a complete verification solution for the most demanding mixed-signal SoC designs.

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