Synopsys TestMAX CustomFault

Redefining Analog Fault Simulation for Automotive Functional Safety and Test Coverage Analysis

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Introduction

The growth in safety-critical applications has ushered in a paradigm shift in automotive IC functional safety and test coverage analysis. The increased need for safety, low defect rate, and long-term reliability is driving automotive IC designers to augment expert judgment with systematic fault simulation, to ensure a high degree of confidence in their analysis and to comply with the stringent automotive standards. However, they are unable to perform fault simulation campaigns at the subsystem and full-chip level due to simulator performance and capacity constraints. Synopsys TestMAX CustomFault™ is a new simulator that features industry-leading CustomSim™ and FineSim® simulation technology and Adaptive Weighted Random Sampling (AWRS) technology to deliver unparalleled analog fault simulation performance, enabling subsystem and full-chip- level analog fault simulation. Synopsys has partnered with industry leaders to develop a solution that is tailored to meet the needs of the automotive industry.

Need for Analog Fault Simulation

The increased need for safety requires automotive ICs to be more robust and resilient. As a result, IC designers must ensure that their designs are fail-operational, have low defect rates, and operate reliably over a long period of time. This paradigm shift has served as a catalyst for change, forcing automotive IC designers to use systematic fault simulation, including analog fault simulation, to augment traditional verification flows, and deploy new verification flows to meet these stringent requirements.

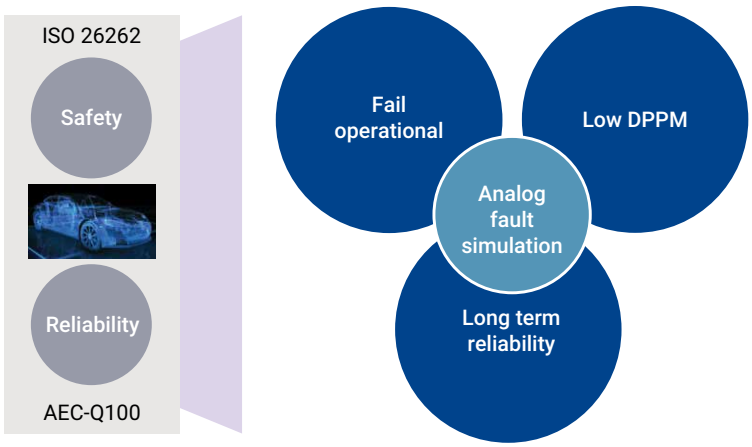

Figure 1: Need for Analog Fault Simulation

Specifically, there are three primary applications that are driving the need for analog fault simulation:

- Automotive functional safety verification
- Manufacturing test coverage analysis
- Silicon failure analysis

Automotive Functional Safety Verification

According to a 2018 PwC study, by the year 2030 40% of mileage in Europe could be on autonomous vehicles while 55% of all new car sales could be electric[1]. The proliferation of safety-critical (ASIL-C/D) applications in automobiles has resulted in more stringent safety requirements (e.g., fail-operational) for automotive ICs, forcing IC designers to revamp existing safety verification flows.

Traditionally, IC designers have relied on expert judgement, assumptions, and a handful of targeted fault simulations to verify functional safety and report ISO metrics, such as SPFM and LFM. But this approach fails to pass the increased scrutiny required for ASIL-C/D applications, driving IC designers to augment expert judgement with systematic analog fault simulation to reliably verify functional safety. (see Figure 2)

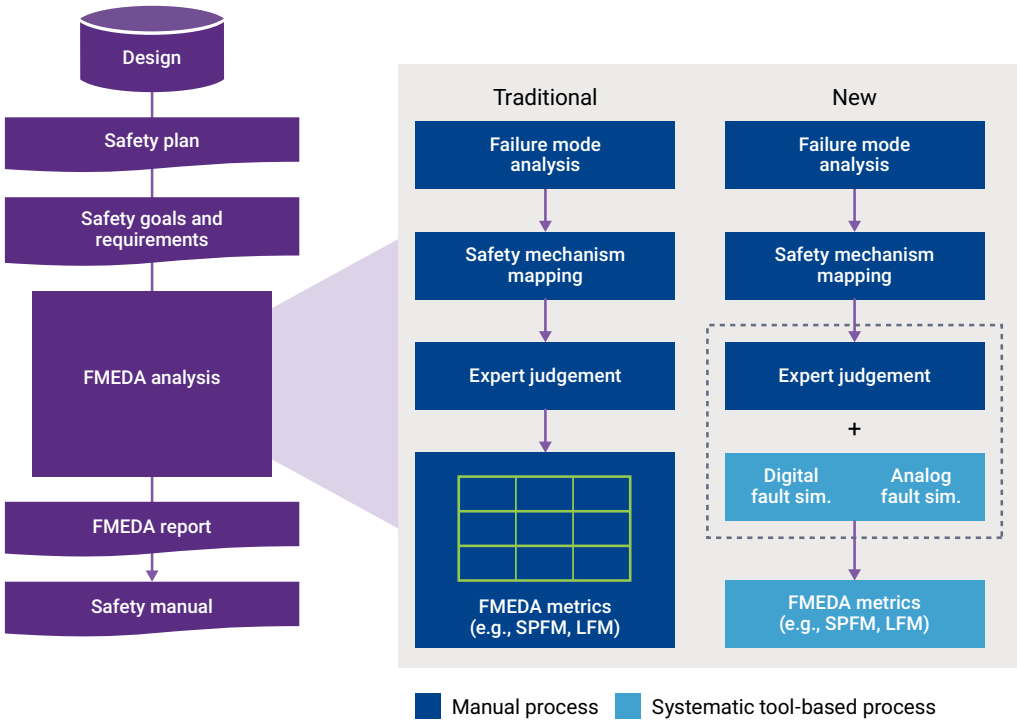

Figure 2: Verifying Functional Safety with Analog Fault Simulation

Manufacturing Test Coverage Analysis

IC designers and DFT engineers have traditionally used digital-centric approaches, such as ATPG and digital fault simulation, to reduce IC defect rates. These approaches result in coverage holes and defect escapes in the non-scan digital and analog portions of the IC and thus are inadequate to meet the stringent low defect rate requirements of automotive ICs. An ITC paper[2] from 2016 indicates that almost 80% of defect escapes are in the analog portions of an automotive IC and this rate is bound to worsen for next-generation automotive ICs with significant analog content.

Therefore, IC designers and DFT engineers are beginning to augment existing test coverage analysis flows with analog fault simulation to plug those coverage holes and reduce IC defect rates (see Figure 3).

1 "Five trends transforming the Automotive industry", PWC 2018

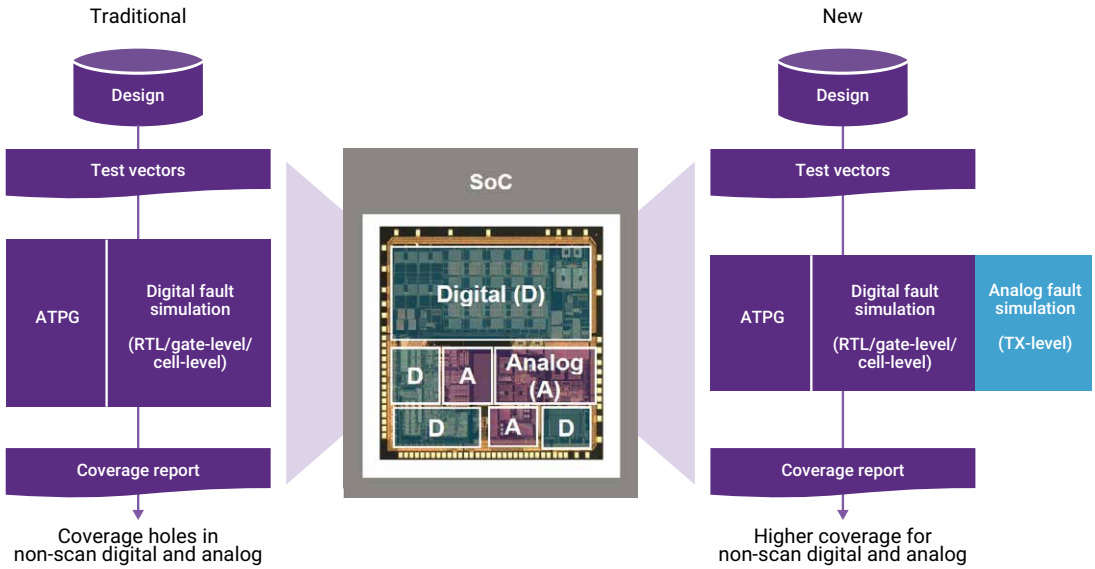

Figure 3: Improving Test Coverage with Analog Fault Simulation

Silicon Failure Analysis

The traditional silicon failure analysis process is both time-consuming and costly, forcing semiconductor companies to adopt novel approaches to optimize the process.

One such novel approach involves using analog fault simulation to root-cause silicon failures in conjunction with a limited silicon failure analysis campaign (see Figure 4). In this approach, failure candidate regions are first identified using silicon debug data, simulation data (e.g., circuit activity), and expert judgement. Then, targeted analog fault simulation is performed on these candidate regions and the simulation results are correlated with the silicon debug data to identify the failing devices.

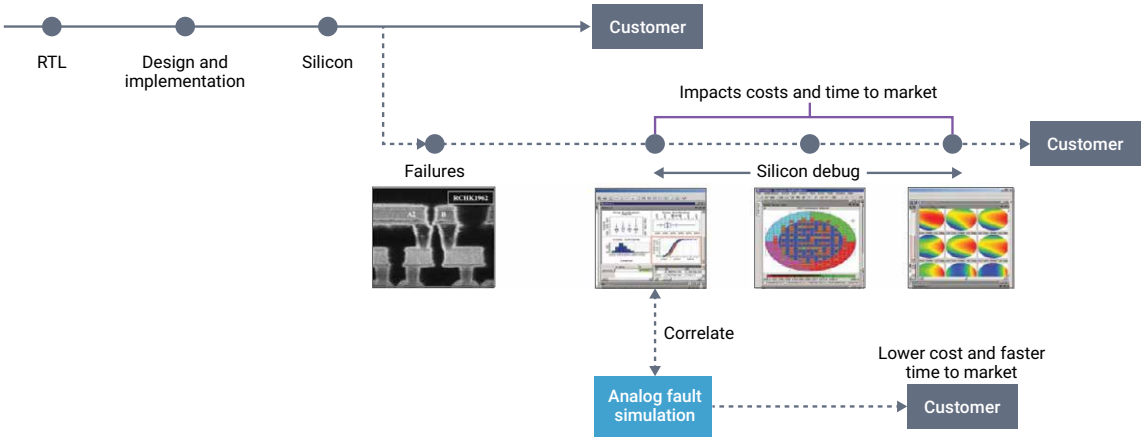

Figure 4: Using Analog Fault Simulation to Root Cause Silicon Failures

Key Requirements for Analog Fault Simulation

The need to comply with the highest safety standards, such as ASIL-C/D, has served as a catalyst for the adoption of commercial analog fault simulation tools at automotive IC vendors. But large-scale adoption has thus far been limited due to simulator performance, capacity, and throughput constraints. Designers are looking to complete subsystem-level fault campaigns within a few weeks to meet their time-to-compliance goals. In addition, ease-of-use features, such as configurable fault models and automatic fault injection, are key care-abouts as they consider scaling their fault campaigns to large block-, subsystem-, and potentially even full-chip-level verification. Finally, requirements such as ISO metrics reporting and multi-testbench grading are essential to enabling designers to meet the unique requirements of automotive functional safety verification and test coverage analysis use cases.

Synopsys Solution—TestMAX CustomFault

TestMAX CustomFault is a new high-performance analog fault simulator from Synopsys. Built on industry-leading CustomSim and FineSim simulation technology and featuring a highly-differentiated feature set (see Figure 5), TestMAX CustomFault delivers superior performance, capacity, and throughput, and advanced ease-of-use and diagnostics that allow users to scale their fault campaigns to subsystems and full-chip in a cost-effective manner.

Figure 5: TestMAX CustomFault Value Proposition

Breakthrough Performance and Throughput

TestMAX CustomFault is built on a modular architecture that fuses the industry's leading CustomSim and FineSim simulators with a powerful front-end to provide seamless fault identification, reduction, simulation, and report generation with unparalleled performance. The flexibility to pick from two leading simulators (see Figure 6) allows designers to reuse existing simulator-specific settings and optimizations.

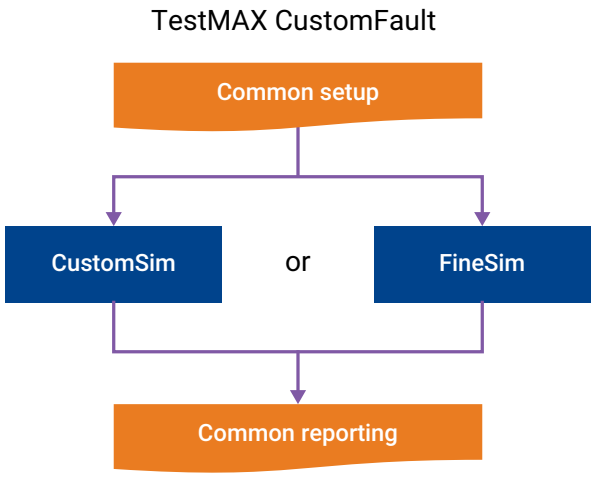

Figure 6: Industry-leading Simulation Technology

TestMAX CustomFault also features the innovative Adaptive Weighted Random Sampling (AWRS) technology that enables random sampling based on built-in or user-defined fault likelihood to reduce the number of fault simulations by several orders of magnitude (see Figure 7). The AWRS technology is critical to enabling practical and cost-effective fault campaigns at the subsystem and full-chip level where the default fault universe can consist of millions of potential faults.

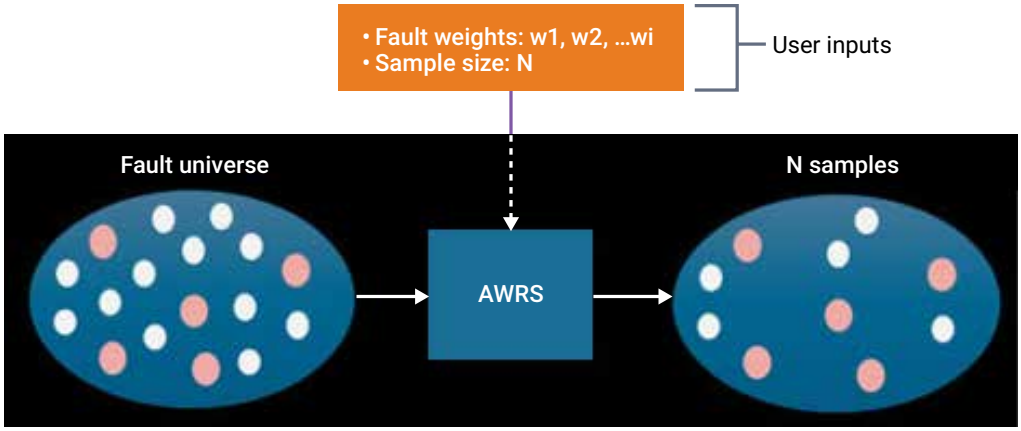

Figure 7: Adaptive Weighted Random Sampling

TestMAX CustomFault is integrated with Synopsys' VCS® simulator to allow users to assess the impact of transistor-level faults on a mixed-signal subsystem. The combination of the fastest transistor-level and digital simulators provides the industry's highest performance and throughput for mixed-signal fault simulation. Users can further improve performance and throughput by selectively injecting faults within a block or excluding certain blocks from fault injection. TestMAX CustomFault also supports distributed simulations with robust job scheduling and seamless failed job recovery, enabling designers to achieve high throughput for large designs.

Superior Ease-of-Use

Ease-of-use becomes a critical requirement as users begin to scale their fault campaigns to multiple large designs involving multiple testbenches. TestMAX CustomFault simplifies fault modeling by supporting a broad class of user-configurable fault models, including traditional short and open models for MOS, R, L, C, and BJT, as well as transient and parametric faults. TestMAX CustomFault also offers a seamless one-step simulation flow that encompasses fault identification, fault reduction, fault injection, parallel simulation, fault detection, and report generation, all while operating off the user-provided "fault free" netlist (see Figure 8). Users can selectively configure each of these steps and execute a custom flow, if required.

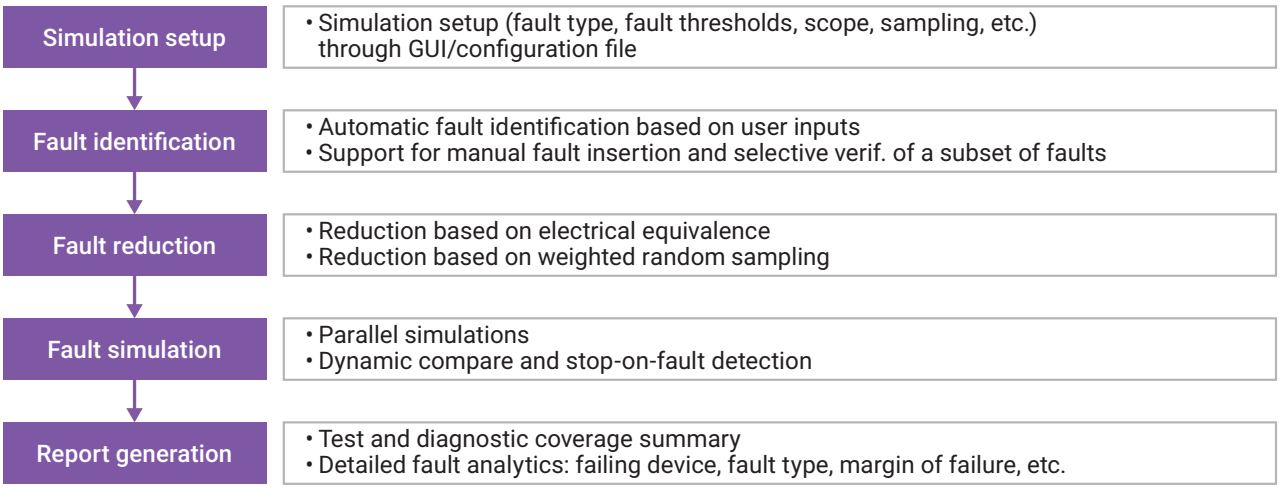

Figure 8: Fault Simulation Flow

Users can efficiently grade multiple testbenches either manually or automatically using the multi-testbench flow. The flow allows users to pick either the default fault universe or a user-defined fault list (see Figure 9) and provides a consolidated set of coverage results and fault analytics for the entire campaign.

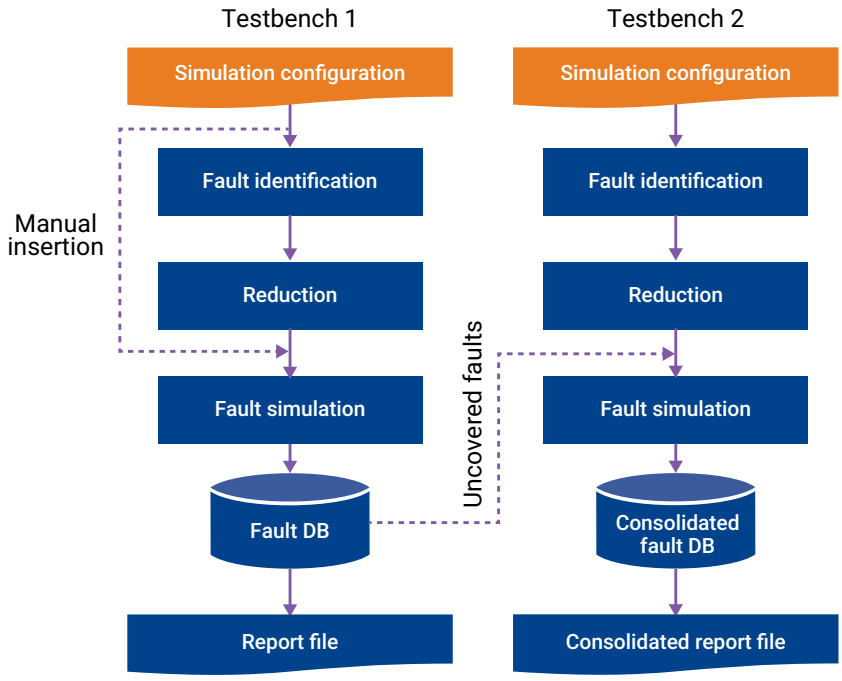

Figure 9: Multi-testbench Flow

To cater to the varied needs of the user, TestMAX CustomFault supports both a GUI-mode and a batch mode. The built-in full-function GUI streamlines simulation setup, launch, and debugging, allowing users to scale their fault campaigns with ease (see example in Figure 10).

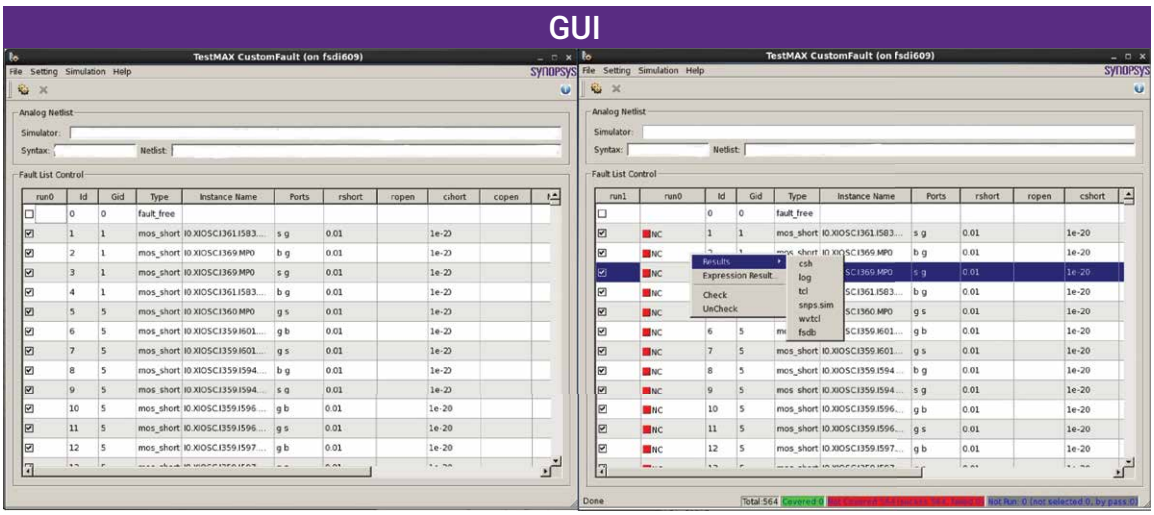

Figure 10: Built-in Full-Function GUI

For batch mode users, TestMAX CustomFault provides an intuitive command file interface that allows them to easily configure the fault simulation. In addition, users can express fault weights as a function of an exhaustive set of model and instance parameters through simple user-defined equations to improve the sampling efficiency of the AWRS algorithm (see example in Figure 11).

```
////////// CUSTOM WEIGHT CODE GOES HERE //////////
double weight=1.0;

weight = 0.5 * w * l * 1e12;

return weight;
}
```

```
////////// CUSTOM WEIGHT CODE GOES HERE //////////
double weight=1.0;

weight = w * l * 1e12;

return weight;
}
```

Figure 11: Specifying Fault Weights as Functions of Model/Instance Parameters

Advanced Diagnostics and Reporting

TestMAX CustomFault caters to the unique diagnostics and reporting requirements of automotive functional safety verification and manufacturing test coverage analysis use cases. Users can analyze the efficacy of primary and redundant safety mechanisms in mitigating failures in their safety-related hardware and generate ISO 26262 metrics such as Diagnostic Coverage for residual faults (DCrf) (see Figure 12) and Diagnostic Coverage for latent faults (DCmpf,l). These metrics can then be used to calculate the Single Point Fault Metric (SPFM) and Latent Fault Metric (LFM) to verify ISO 26262 compliance. The diagnostic coverage metrics can also be automatically imported into Synopsys VC Functional Safety Manager (VC FSM) to enable SPFM and LFM roll-up for multiple designs as part a broader Failure Mode Effects and Diagnostics Analysis (FMEDA) campaign.

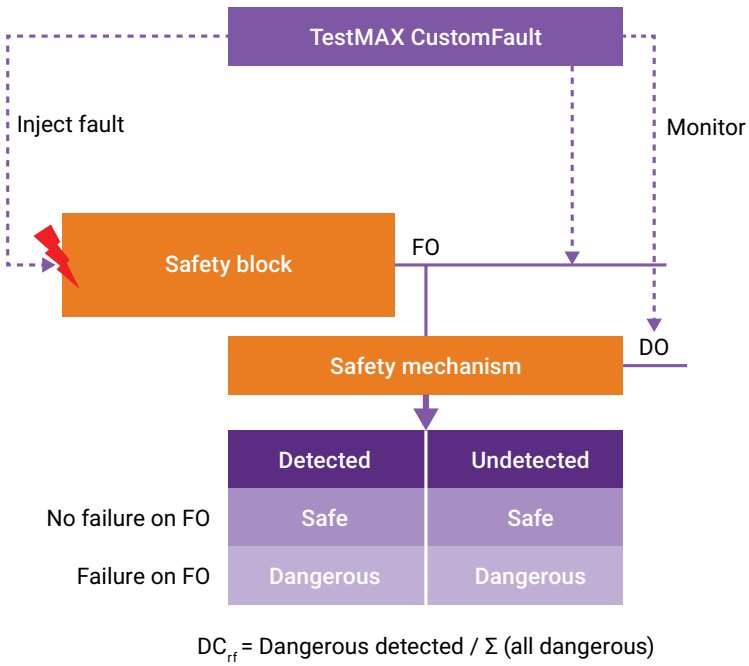

Figure 12: Calculating Diagnostic Coverage for Residual Faults (DCrf)

For users performing test coverage analysis, TestMAX CustomFault provides a consolidated set of coverage results including per-testbench/per-fault analytics across multiple testbenches (see Figure 13). In addition, TestMAX CustomFault orders testbenches based on incremental coverage improvement, allowing users to quickly assess, modify, and re-order the test sequence to meet desired coverage targets (see Figure 14).

```
                        TestMAX CustomFault
       Version P-2019.06-SP1-20190823 - Aug 23 2019 02:21:41 5763457

       Tags    Sample-Size
    DropOut           600
 funcTestMax          600
 funcTestMin          600

*DEFECT UNIVERSE SUMMARY
   mos_mac_open                  4311
   mos_mac_short                 4078

         TOTAL                   8389

*COVERAGE SUMMARY
Defects covered - unweighted (covered/simulated):
          Type                DropOut             funcTestMax             funcTestMin

   mos_mac_open               25/338                24/338                34/338
   mos_mac_short             194/643               220/643               226/643
         TOTAL               219/981               244/981               260/981

Defects covered - weighted (covered/simulated):
          Type                DropOut             funcTestMax             funcTestMin

   mos_mac_open         44.3269/516.224         75.2444/516.224          60.9/516.224
   mos_mac_short        157.309/450.494         189.453/450.494        198.455/450.494
         TOTAL          201.635/966.719         264.698/966.719        259.355/966.719

Weighted test coverage:
        DropOut                20.86%  (sample size: 600)    (95% Confidence Interval: 20.86±2.18%)
     funcTestMax               27.38%  (sample size: 600)    (95% Confidence Interval: 27.38±2.38%)
     funcTestMin               26.83%  (sample size: 600)    (95% Confidence Interval: 26.83±2.37%)

TOTAL Coverage:
      Sampled[*]               32.75%  (sample size: 600)    (95% Confidence Interval: 32.75±2.5%)
```

Figure 13: Consolidated Coverage Report Example

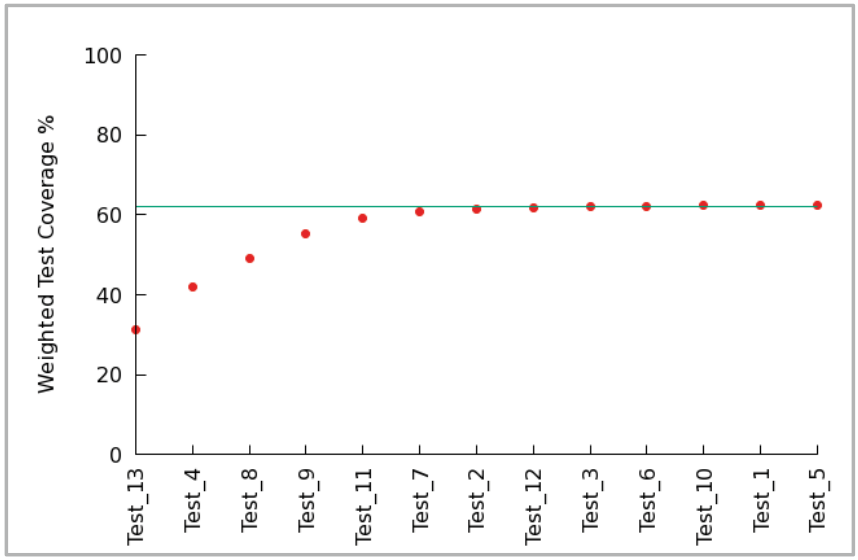

Figure 14: Ordering of Testbenches Based on Incremental Coverage Improvement

Summary

TestMAX CustomFault simulator is a breakthrough new product for analog fault simulation that was built with the singular objective of making subsystem- and full-chip-level fault simulation practical. Featuring the industry's leading simulation technology and a highly differentiated feature set, TestMAX CustomFault is set to redefine analog fault simulation for automotive functional safety and test coverage analysis.

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