SYNOPSYS®
Accelerating Innovation

ZeBu Success Story
CSR Image Processing

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With ZeBu we achieved a win-win situation: not just faster time-to-market for our chips, but also faster time-to-market for the products of our customers. I would say confidently that with ZeBu we were able to cut close to three months off the development cycle of our image processing SoCs."

CSR

Mark Busa
Director of ASIC Engineering for the Imaging Group at CSR

CSR Background

CSR is a leading developer of silicon and software for the consumer electronics market, specializing in imaging, connectivity, location, voice and music, and automotive infotainment. The imaging division supplies the critical system-on-chips (SoCs) to drive end-products that produce images, including printers, scanners, copiers, fax machines and multi-function printers.

Our SoCs comprise multiple microprocessors, including ARM11MPCore® and Cortex M3®, CSR proprietary DSP cores, and multiple interfaces, such as USB interfaces, PCIe interfaces and SATA interfaces. In addition, these devices contain proprietary interfaces to the scanner engine and to the printer engine, as well as DDR interfaces to DDR memories. See Figure 1.
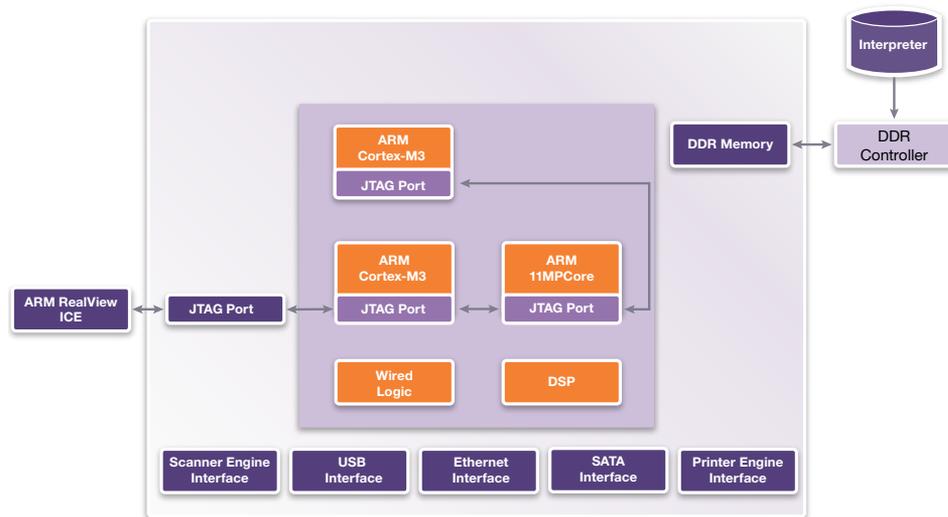

Figure 1: CSR's SoC Block Diagram

A scanned image undergoes a great deal of image processing before print out, from noise removal, to color correction, to color conversion from red-green-blue to cyan-magenta-yellow, and so on. The image processing is done partly in hardware and partly via software algorithms executed on the embedded digital signal processor (DSP) cores, such as image scaling, rotating, and the like. The complexities of our SoCs range up to tens of millions of ASIC-equivalent gates. The designs further embed an operating system such as Linux.

A very critical component in the deployment of these SoCs in a printer/scanner is a software program called "interpreter". The interpreter translates the commands embedded in the PostScript files sent by a PC to a printing device into actions that SoC chip perform on the images before printing or scanning them.

CSR's Verification Flow and Challenges

Our design flow starts at the register transfer level (RTL), with RTL verification based on Synopsys' VCS and another simulator. But given the complexity of the chips, real-time or quasi-real-time image processing cannot be performed via HDL simulators alone.

Until a few years ago, system integration of the hardware with the embedded software was carried out on first silicon from the foundry.

In one occasion, it so happened that we tried to run our interpreter on the engineering samples we got from the foundry and the chips failed. The interpreter found a bug in our chip. Needless to say, fixing bugs post-silicon is a very expensive proposition, not to mention the dramatic financial impact on our customers once the chips are delayed by several months. That was the trigger that prompted an investigation in the hardware-assisted verification field, and led us to adopt an emulation platform.

CSR Selects ZeBu

After an internal analysis, we chose ZeBu® Server-1 as our hardware assisted verification platform. The main factor that most influenced us was ZeBu's fast execution performance that enabled us to run the interpreter on the designs ahead of silicon, which was an absolute requirement. We also valued the automatic compilation process of ZeBu and its automatic partitioning across multiple FPGAs.

ZeBu Results

We use ZeBu Server-1 for system level verification when the RTL design reaches stability. ZeBu can typically achieve an execution speed of 3 to 4 megahertz, and at this speed we can execute our interpreter on the design mapped inside the emulator and process tens of thousands images, testing all possible parameters, 24/7 for several weeks.

The biggest advantage ZeBu gives us is the ability to detect bugs deeply embedded in the design that can be detected only by processing real world images under all possible conditions.

What is likewise very important is that our customers—the printer/scanner companies—also use the same ZeBu configuration to test their own software on the RTL designs we deliver to them ahead of silicon. They can run their code early on in their development cycle, thus achieving significant confidence before tapeout that they will meet their design specifications.

Today, our customers have an early software development platform for an early start of their software verification and we at CSR have an effective verification platform that allows us to run our applications on our own chips.