SYNOPSYS®
Silicon to Software™

Test Evolution's Success With VCS and Verdi

Delivers Faster Verification Closure on Next-Generation FPGA-Based Post-Silicon Validation Products

> *"After an extensive evaluation of available functional verification solutions, we selected the combination of VCS simulation and Verdi debug for our next generation design. The combination of VCS performance and native integration with Verdi, delivers a solution that is intuitive, easy to use and gives us the confidence to meet our tight time-to-market windows."*—*Al Czamara, VP Engineering, Test Evolution Corp.*

About Test Evolution

Test Evolution Corporation (TEV) develops post-silicon validation and IC manufacturing test (ATE) products, engineering services and systems for semiconductor R&D and manufacturing. TEV's post-silicon validation products are based on its Test IP and Intelligent Peripheral Instruments platform, supporting protocols such as MIPI CSI and DSI, D-PHY, C-PHY, HDMI, and USB for single and multi-protocol functional test. Its ATE products include AXIe standard chassis and instruments, digital and RF subsystems, device power source and precision measurement units.

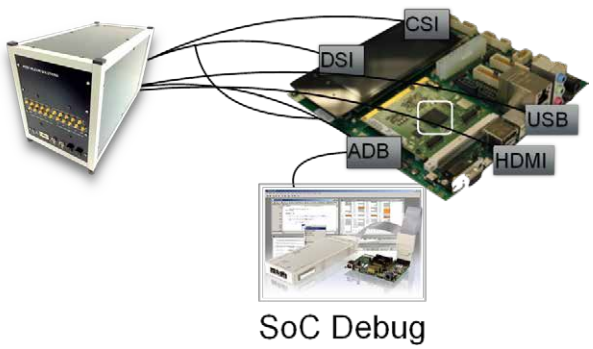

Figure 1. TEV's post-silicon validation system

Challenges

- Perform functional verification of large next-generation FPGA designs in short product windows
- Simultaneously perform complex debug tasks with multiple design experts
- Reduce debug turnaround time (TAT), especially for long simulation run times
- Achieve coverage closure with UVM and in-house verification methodologies

Simulation and Debug Solution

- Synopsys VCS solution for industry leading simulation and constraint solver engines
- Synopsys Verdi industry-standard debug solution for advanced debug automation

Benefits

- Natively integrated simulation and debug enables fastest simulation and debug TAT in the industry
- Innovative Verdi debug capabilities
- Complete solution for coverage-driven methodologies

Overview

TEV recently announced the MIPI DSI-2 with C-PHY (and D-PHY) protocol test instrument, built on an FPGA from Xilinx (a Synopsys strategic partner). To meet the tight time-to-market (TTM) schedules of their customers, TEV's products needed to adhere to similarly tight deadlines.

Typically, TEV engineers work on large designs requiring long simulation runtimes. Debug of any design issues require multiple collaborations, simulation and debug iterations. TEV needed a solution that could address these challenges.

Accelerated SoC Verification Closure

To address the issues of long simulation runtimes and multiple debug iterations, TEV leveraged Synopsys' VCS simulation and Verdi debug solutions for verification of MIPI DSI-2.

MIPI DSI-2 was designed and modeled in SystemVerilog and verified using Truss/Teal, a UVM-like methodology. After TEV and Synopsys discussed the issue of long simulation runtimes, it was identified that the large testing space (not all relevant to the design), was adding the additional time. As a result, Synopsys recommended TEV utilize VCS advanced constraint solver technologies into the methodology. By doing so, TEV was able to speed up simulation time by almost two-fold, shortening the overall verification cycle.

To enhance overall debug productivity, TEV engineers needed a verification solution that was easy-to use, delivered end-to-end integration over multiple phases of verification and enabled faster turnaround times. TEV selected Synopsys' Verdi debug solution because of its unique and innovative debug capabilities such as Reverse debug, 'What-if analysis' and Adaptive Exclusion — all tightly integrated with VCS.

On the MIPI DSI-2 project, TEV engineers used Verdi's software-oriented debug approach for SystemVerilog and UVM testbenches to effectively explore, debug and optimize their hybrid testbench environment. With Verdi and VCS's Reverse Debug capability, they could quickly move backward in time within a simulation and avoid multiple simulation and debug iterations. With 'What-If Analysis', they were additionally able to fix and validate their testbench, all within a single simulation run. Unlike the competition, Verdi is a unified debug environment for design as well as testbench debug. This enabled TEV's design and verification teams to collaborate easily and productively.

TEV engineers' familiarity with the Verdi interface enabled them to quickly ramp up on Verdi's integrated verification planning and coverage analysis. Specifically, the automated adaptive exclusion flow saved TEV several days of manual effort as they approached coverage closure. Faster simulation, more productive debug and seamless integration of various verification activities enabled TEV to meet design quality goals faster and accelerate time-to-market. With the native integration of verification planning, simulation, debug and coverage data in Synopsys VCS and Verdi, Synopsys became the verification solution to address TEV's growing verification challenges.

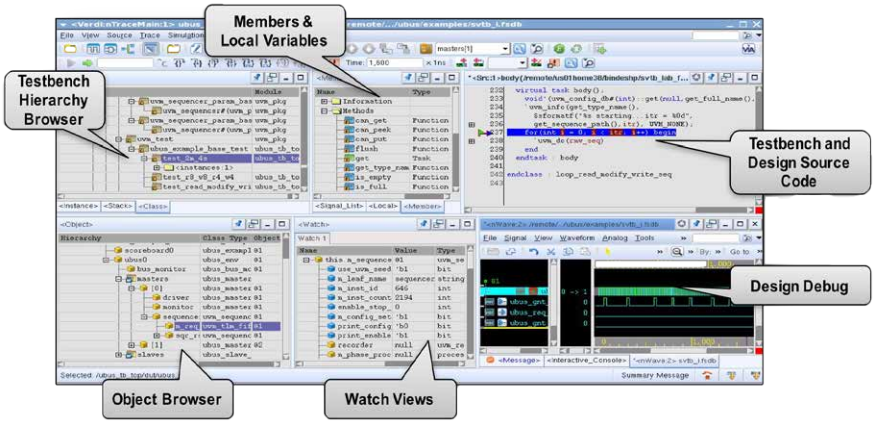

Figure 2. Unified Design and Testbench Debug in Verdi

Conclusion

Before starting the MIPI DSI-2 project, one of the major business challenges for TEV was meeting their customer's schedule, while maintaining the quality of the product. TEV's adoption of Synopsys' verification solutions played an important part in building confidence about in-time delivery of MIPI DSI-2. TEV was able to commit to the timely delivery of the product due to two values — the superior technological solution from Synopsys and the responsive and expert support during the project. Synopsys' support had been critical to ensuring TEV meet their tight schedule and achieve their verification goals in time.

> *"Synopsys' technical support is excellent. The team is not only prompt but also thorough and insightful. Their experience clearly comes from the verification of the industry's most complex designs."*
>
> *—Al Czamara, VP Engineering, Test Evolution Corp.*