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Predictable Success

Synopsys and Stellamar

All-Digital ADC a Design Success with SPW Algorithm Design Tool

Synopsys is a key partner in helping us innovate. Synopsys SPW gives us the ability and confidence to focus on what differentiates our product and gets us to market faster."

Stellamar
Digital solutions for an analog world

Allan Chin
CEO, Stellamar

Business

Stellamar is an innovative design engineering leader in the creation and distribution of valuable IP solutions that enable analog functions to be implemented in a digital environment.

Challenges

- Needed fast time-to-market
- Needed to know the design would be functionally correct the first time with no respins
- Wanted a common testbench for both algorithm and gate-level timing simulations

System-Level Design Solution

- SPW model-based algorithm design tool

Benefits

- Achieved an integrated design flow from concept to RTL implementation
- Applied common testbench throughout the design process with an integrated verification flow
- Proven reliability and stability delivering first time success

Overview

Stellamar has pioneered the development of a new Digital ADC (analog-to-digital converter) technology that can be implemented in a digital silicon technology without using any of the analog IP blocks traditionally used for ADC designs. This technology reduces the design cycle time and cost of ADCs integrated in ASICs, and can be implemented in fully digital microchips such as FPGAs avoiding the use of costly external ADCs and saving board space.

SPW was used extensively to model, simulate and verify the algorithm for the ADC. Once verified, Stellamar used SPW HDS (hardware design system) to generate synthesizable RTL code for a power and area optimized fully digital synthesizable ADC. The ADC can then be implemented in either FPGAs or ASICs. As part of this development, Stellamar also built a prototype for the feasibility study and demo boards that highlighted the flexibility and performance of their all-digital ADC solution.

We need a solution that gives us both an integrated implementation and verification flow. The ability to use a common SPW testbench throughout the design process ensures functional correctness throughout our design."

Luciano Zoso
CTO, Stellamar

For the demo boards, ancillary pieces of hardware were also designed using the SPW HDS design flow. This included an S/PDIF encoder which allows users of the FPGA board to have a single-wire connection at the output of the ADC.

Leading Algorithm Design Solution

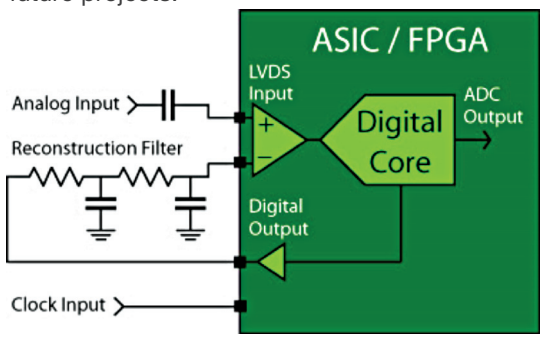
The ADC is suited for voice, high-quality-voice, and sensor applications. Stellamar's ADC is particularly appealing to portable applications where area, weight and power consumption are at a premium. Also, due to the all-digital architecture, it can be made rad-hard through any radiation hardening CMOS process.

Stellamar's top challenges for this complex design revolved around creating integrated design flows from algorithm to implementation and verification. To reduce time-to-market and stay competitive, the company needed a proven technology that gave them predictability and enabled first-pass success.

Using Synopsys' SPW algorithm design tool, Stellamar quickly created a model to simulate the algorithm, extending all the way to a bit-true functional reference model. They were then able to link to FPGA synthesis tools and RTL verification tools – a flow well supported by SPW HDS. By reusing the same system testbench throughout the design, from concept to bit-true modeling to RTL code, Stellamar had high confidence in the functional correctness of the design.

Stellamar's previous experience with SPW made the choice to use SPW for this design project easy. The design team found SPW very easy to integrate because the same design environment could be used for almost all tasks. Based on the predictable output of the tool and the expert support of Synopsys' field application engineers, the design team knew they would be able to focus on the differentiating aspects of their complex design while achieving reliable results.

So far ADCs have been unchallenged strongholds of the analog design, but with the help of Synopsys tools Stellamar has turned digital ADCs into a reality, thus changing the way ADCs are designed forever. Stellamar plans to continue using SPW in future projects.



Block Diagram of Stellamar's Digital ADC

"SPW's model-based approach to algorithm design makes modeling, simulation and verification much faster and easier. We know we can count on SPW to get us to reliable, synthesizable RTL code faster than any other tool.

Luciano Zoso, CTO, Stellamar

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