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SPW Enables 3-4x Faster Algorithm Design Flow for Modem Design

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Naohiko Iwakiri
Senior Research Scientist of Tokyo University, and Institute of Space and Astronautical Science, JAXA

Business

The primary mission of the Institute of Space and Astronautical Science (ISAS) within the Japan Aerospace Exploration Agency (JAXA) is to advance space science in Japan. Through collaboration with universities, ISAS conducts scientific research in outer space contributing to JAXA's and Japan's entire space development efforts.

Challenges

- Design optimal, low power, high-speed modems for nano satellites in future satellite applications
- Develop DSP algorithms and FPGA designs rapidly
- Improve productivity with a model-based approach

System-Level Design Solution

- SPW algorithm design tool and model libraries
- SPW model wizard integrates existing C/C++ code

Benefits

- Get to results faster with the fastest simulation, deploying low-cost PC clusters
- Access to high quality signal-processing model libraries, including models of non-ideal RF devices
- Provide an intuitive and easy-to-use interface between blocks with model-based approach

Overview

This specific ISAS R&D team is a long time user of the SPW algorithm design tool and models. For their latest project, the team needed to develop a fast (~250M symbols/sec), low power modem for a nano satellite (<100kg) downlink communication system, to be deployed in future satellite projects.

Since the R&D team is a small group, they need an effective design approach. Access to reliable model libraries supporting the latest communication concepts such as OFDM and MIMO, and also the ability to integrate customer-coded functionality written in C/C++ are mandatory to accomplish this type of complex design. Additional requirements include tool support to eliminate re-designs when interfacing between blocks or reusing previous block versions. In addition, the team requires fast simulation in order to optimize across many scenarios. Finally, they need to efficiently transfer the system-level description into an FPGA circuit.

Leading Algorithm Design Solution

The R&D team estimated that it would take a long ten to twelve months to develop all the blocks required for the modem design if designed from scratch using C or C++.

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They also wanted to avoid the tedious rework caused by the different skill sets and preferences of each designer working on the project. In addition, they needed a development environment which would allow them to seamlessly implement their algorithm on FPGAs.

SPW eliminated these issues by providing an intuitive and easy-to-use interface between blocks. Because SPW provides a common simulation and verification environment with a model-based approach, diverse teams working on a single project could get to system-level simulation results faster.

Interfacing to different blocks being designed by different people can sometimes cause hard-to-debug problems when a different version of a block is used. SPW's built-in data management and version control system eliminates these issues by isolating the design environment of each team member.

Besides offering the fastest simulation, SPW's built-in facility to distribute simulations over PC clusters also contributed to a significant reduction in development time. "SPW is the ideal tool for small teams working on big projects requiring a lot of simulation, since PC clusters are easy to construct without MPI programming. Furthermore, SPW's link to MATLAB allows our student researchers to use MATLAB for analysis and visualization of simulation results," said Naohiko Iwakiri, senior research scientist for ISAS. "Designing an optimal system in the shortest amount of time, with minimal effort and labor costs, is the biggest benefit that SPW provides. It would probably take 3-4 times the effort without SPW to model all simulation scenarios, from initial concept studies all the way to a fixed-point reference."

High-Quality Models and Support

In order to maintain competitiveness in space communications, this ISAS R&D team needs to quickly produce modems optimized for nano satellites which have to function in the harsh environment of outer space. These modems require the latest communication concepts such as OFDM, MIMO, but also address timing imperfection, phase noise, linear/non-linear distortion owing to a power amplifier and other RF devices. "It would be impossible for a small team to develop such a highly reliable library and flexible system design approach in the timeframe required for our projects," said Naohiko Iwakiri.

The quality and breadth of Synopsys' model libraries and the expert knowledge of the model developers greatly eased the design process while ensuring high quality of results. Access to more than 3000 models, all available in source code and highly parameterizable, enabled the team to focus on differentiating their algorithmic concepts from the very beginning.

In the next phase of the design, the ISAS R&D team will take advantage of SPW's ability to offer the fastest refinement of floating-point algorithms into fixed-point algorithms for an FPGA implementation. Synopsys' other tools, such as Synphony, Synplify, and VCS will accelerate FPGA development. With this design project moving ahead in record time, the ISAS R&D team is well on its way to supporting the next generation of reliable, high-speed and low-power communication systems for nano satellites and deep space missions.

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