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Synopsys and Kyushu Institute of Technology (Kyutech)

Computer Science Team Uses HAPS to Demonstrate a Unified Verification Framework – Wins Demonstration Award At APCCAS

"Our research group required a prototyping platform to confirm signal processing algorithms of a new Wireless LAN design. Synopsys HAPS allowed our team to successfully conduct hardware/software co-verification to confirm feasibility and demonstrate operation of new WLAN system circuit designs."

Dr. Hiroshi Ochi
Professor, Computer Science and Engineering at Kyushu Institute of Technology (Kyutech)

Academic Research

Kyushu Institute of Technology (Kyutech) is a 100 year old science and technology institution with campuses in Tobata, Iizuka, and Wakamatsu in Fukuoka Prefecture Japan. At Kyutech's Department of Computer Science and Electronics, the curriculum and research integrate: electronics engineering dealing with semiconductors and electronic circuits, computer engineering for the fundamentals of computers and their application technologies, and telecommunication engineering represented by the Internet and mobile phones. Research into MIMO radio transceivers of IEEE 802.11ac WiFi applications by the Computer Science department has led to use of FPGA-based prototypes to confirm algorithm function and characterize performance.

Challenges

- Demonstrate circuit operation of WLAN transceiver system with a variety of system parameters including: frame format, channel bandwidth, and FFT length
- Generate performance results using WLAN metrics such as constellation point, Bit Error, and Packet Error Rates
- Validate new WLAN receiver block algorithms based on DSP processing test vector data produced by MathWorks MATLAB
- Support long validation periods at multi-megahertz performance
- Establish a physical connection between a host workstation and the FPGA-based prototype for stimulus, control, and monitoring
- Support software-driven tests to interface to the live prototype system

Synopsys Solution

- Synopsys HAPS® FPGA-Based Prototyping System providing multi-million ASIC gate capacity
- Synopsys Synphony Model™ Compiler (SMC) for model-based RTL design
- Universal Multi-Resource Bus (UMRBus®) Interface Kit for host workstation connection and API for software interfacing to design-under-test (DUT)

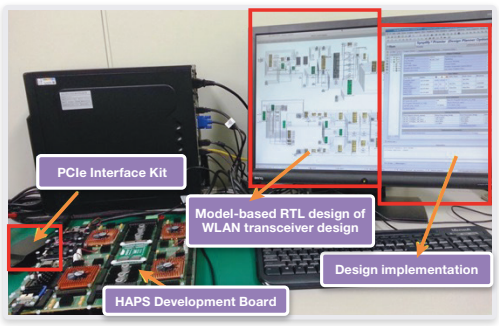

Figure 1: Kyutech WLAN transceiver system demonstrator and validation platform using HAPS FPGA-based prototyping system

Overview

Kyutech's research team has developed a novel demonstration and validation platform that connects MATLAB's test stimulus and analysis features with the HAPS system for FPGA-based prototyping in order to demonstrate WLAN transceiver system design.

The demonstration system illustrated above begins with the Simulink / MATLAB model-based design environment to develop new DSP processing algorithms. The Synphony Model Compiler provided the automation to synthesize the electronic system-level algorithms for the FPGA-based prototype. Simulink / MATLAB also produced the test vectors for the receiver block to confirm operation of the prototype transmitter. The data vectors are sent to a HAPS system platform through a high-bandwidth, HAPS UMRBus, PCIe-over-cable connection. The data transfer is performed by a software application based on a C/C++ program and the UMRBus application programming interface (API). The RX DUT, hosted by HAPS, communicates data transactions with software with UMRBus Client Application Interface Module (CAPIM) interfaces. CAPIM modules pass the received data to appropriate internal FPGA memory.

After the input data is available and enable control signal is activated, the receiver block performs the signal processing task by reading data from ADC RAM and stores decoded data, as PDU format data, in TRX MSDU RAM. When the receiver block finishes its task, the hardware asserts interrupt signal and sends it to the memory and stores in a buffer text file. This result, then, is processed by the MATLAB tool to examine system performance such as BER.

The software flow consists of a scripting program that handles design process and a test bench program that performs the verification process for the test circuit. The test bench software performed control, data loading, and data retrieval for post processing analysis. The test pattern is generated in Matlab and sent to HAPS through the UMRBus.

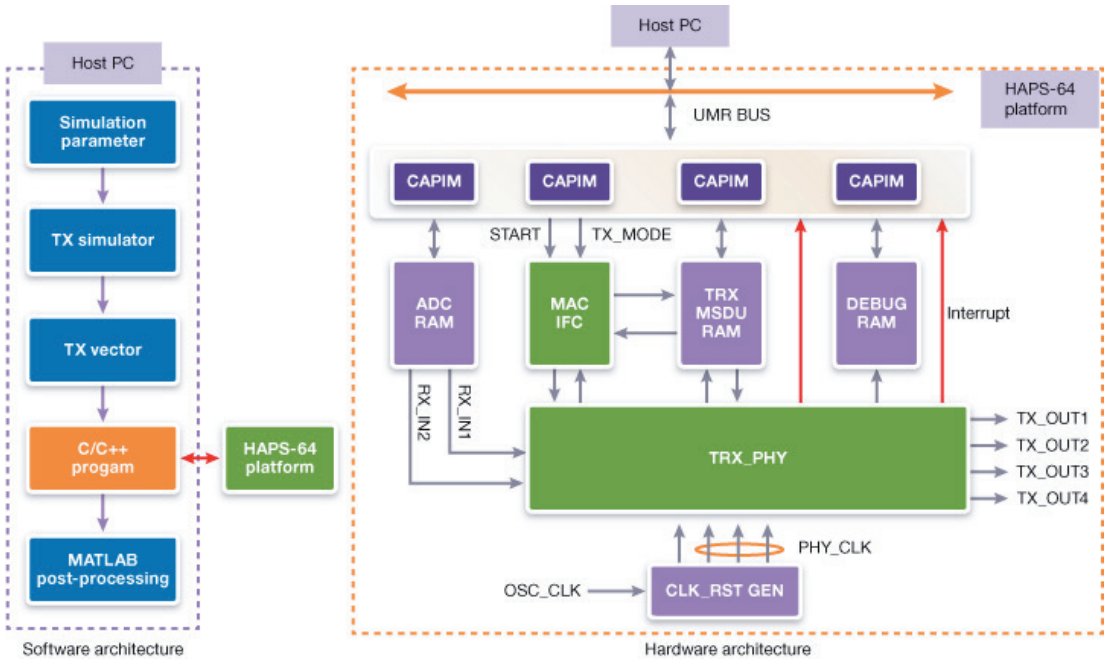

Figure 2: Kyutech HAPS-64 platform based WLAN transceiver demonstrator system architecture

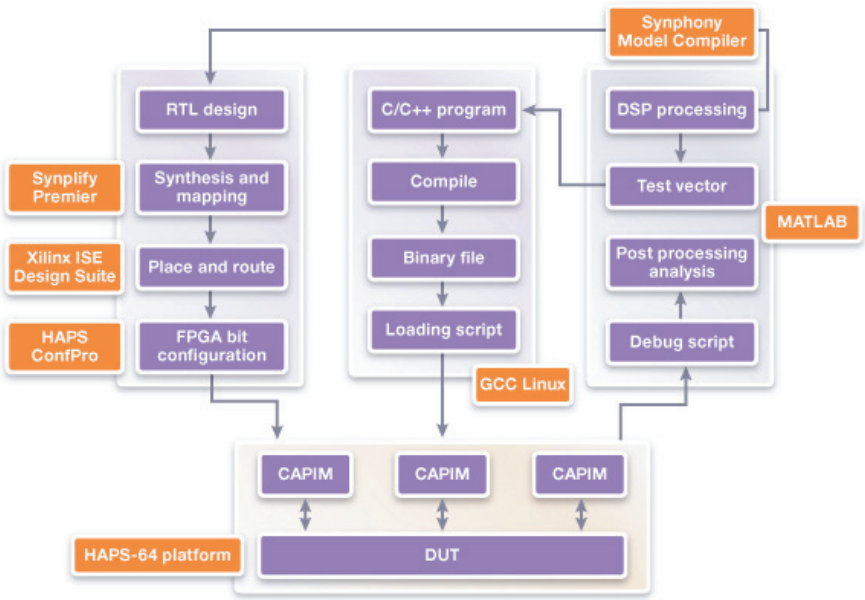

Figure 3: Kyutech hardware software design flow

Meeting the Demand for Performance

Kyutech confirmed that FPGA-based prototypes are feasible for Wireless LAN validation and demonstration:

- Simulink / MATLAB to FPGA design flow with re-programmable prototyping platform for easy implementation of design revisions and architecture variation
- HAPS system prototype delivered processing frequencies of 120 MHz for near real-time performance versus traditional simulation kHz performance
- HAPS UMRBus for workstation connectivity enabled control and monitoring using custom programs written in C/C++

Key benefits included:

- Fast prototype turnaround time allowed the research team to demonstrate quality of results of various processing algorithms
- High performance FPGA synthesis implementation supports data processing at over 100 MHz
- User applications developed to interface with MATLAB data generation and analysis enabled via HAPS UMRBus API
- Scalable hardware capacity and prototype planning automation allows multi-million ASIC gate designs to be prototyped

Award Winning Results

The Kyutech research team took their WLAN demonstration platform to the 2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS). The APCCAS is a major international forum established by the IEEE Circuits and Systems Society for scholars, scientists, educators, students and engineers to exchange their latest findings in circuits and systems. The Poster and Demonstration submission, by Kyutech, won the conference's award for outstanding live demonstration.

Congratulations to the department team: Nana Sutisna, Leonardo Lanante Jr., Yuhei Nagao, Masayuki Kurosaki, and their advising professor, Dr. Hiroshi Ochi!

Figure 4: Kyutech computer science department team

To learn more about Kyutech Kyushu Institute of Technology, visit http://www.kyutech.ac.jp