

Synopsys and Baikal Electronics

SoC Team Applies Synopsys HAPS and AMBA Transactors to Accelerate the Availability of Prototypes and Improve Product Quality



The HAPS-70 proved to be a powerful and easy to use configurable prototyping platform for our multicore MIPS and ARM CPU-based SoC design that integrated a variety of interface IP cores. Together with support from Synopsys we managed to successfully prototype our SoC starting from the early phases of our project.”



Pavel Osipenko

Head of R&D Department, Baikal Electronics

About Baikal Electronics

Baikal Electronics, Moscow, Russia, is a developer of integrated circuits based on MIPS and ARM processor cores. Baikal's multi-kernel SoCs are designed for a wide range of industrial and consumer devices for use in communications, industrial automation and embedded systems markets.

Challenges

- ▶ Establish an executable platform for hardware/software integration
- ▶ Trap errors that occur from hardware/software interactions
- ▶ Support software development as early as possible in the ASIC engineering schedule

Requirements

- ▶ Capacity for >20 million ASIC gates and scalable up to 100 million ASIC gates
- ▶ Flexible to adapt to different styles of IP and SoC configurations
- ▶ Advanced debugging capabilities
- ▶ The ability to mix TLM with RTL prototypes

Prototyping Solution

- ▶ Synopsys Virtualizer™ and Platform Architect MCO tools for TLM-2.0 model integration and packaging
- ▶ Synopsys HAPS® FPGA-Based Prototyping System providing multi-million ASIC gate capacity
- ▶ HAPS Transactor Library for AMBA
- ▶ Universal Multi-Resource Bus (UMRBus) Interface Kit for host workstation connection and API

Benefits

- ▶ Early start of hardware/software integration tasks, before the RTL codebase was complete, using a hybrid prototype approach
- ▶ Found and debugged functional errors early
- ▶ Increased testing between the CPU and other parts of the system improved RTL quality



Figure1: Baikal's Custom HapsTrak 3 Daughter Board with PHYs

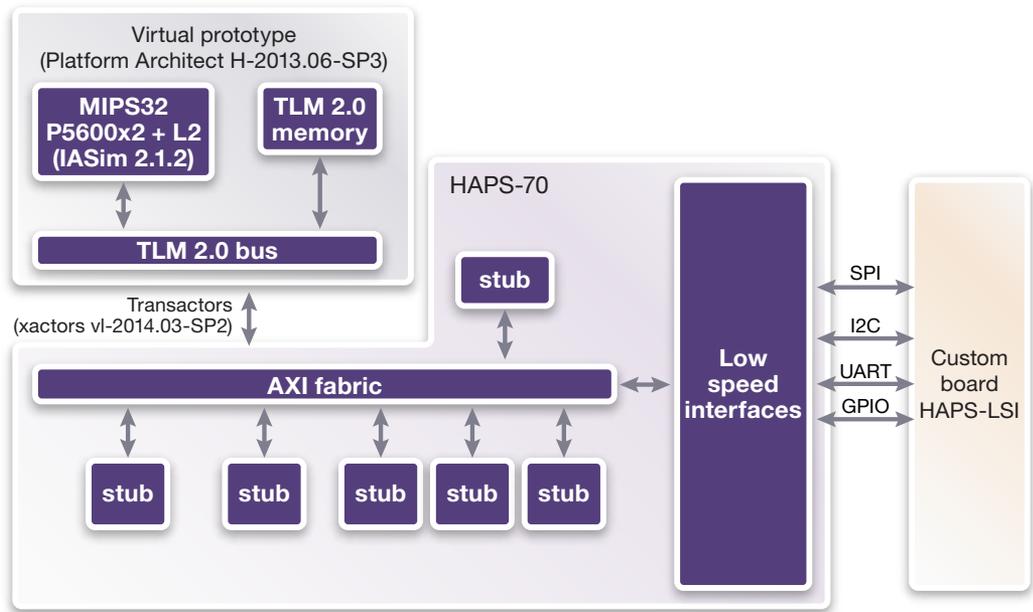


Figure 2: Stage One Prototype - Baikal-T DUT0

Overview

Baikal's new multicore SoC, named Baikal-T, contains a 2-core MIPS P5600 cluster with 1M L2 cache, ARM AMBA fabric, and Synopsys DesignWare® IP: DDR3, PCI Express® 3.0, 10G and 1G Ethernet, SATA 6G, USB 2.0, and several low speed peripherals. To reduce the development and maintenance effort and speed the availability of prototypes for hardware/software integration, the team chose the HAPS-70 Series instead of developing a custom-built FPGA based prototype.

Because of the complexity of the SoC, the team adopted an incremental approach to the prototype bring-up. The team started with a hybrid solution consisting of a virtual prototype with transaction-level models of the CPU and memory subsystem with connections to the RTL version of low-speed peripherals hosted by the physical prototype, HAPS. Then progressively transitioned more and more of the design blocks into the physical prototype.

Multi-Stage SoC Bring-Up

The initial system, DUT0, integrated the MIPS and memory system with SPI, I2C, UART, and GPIO peripherals. High-speed interfaces like PCI Express were stubbed off. The Imagination IASim TLM 2.0 model was integrated with a TLM-2.0 memory and the AMBA AXI interface using Platform Architect MCO and Virtualizer. In the RTL context, the peripheral controller logic and bus interface was established with an interface to a custom-built HapsTrak 3 daughter board containing the high-speed PHYs, switches, headers, and LEDs.

The simple hybrid implementation allowed Baikal to conduct integration and driver development for the peripherals much earlier than they had been able to accomplish in the past.

Next, DUT1, a pure physical prototype, was brought up in one chip using a single MIPS core, cache control, and memory subsystem. A pair of FPGAs hosted the design while a HapsTrak 3 SRAM daughter board provided the memory resource. This simple plan allowed the team to boot Linux and run the CPU at 25 MHz.

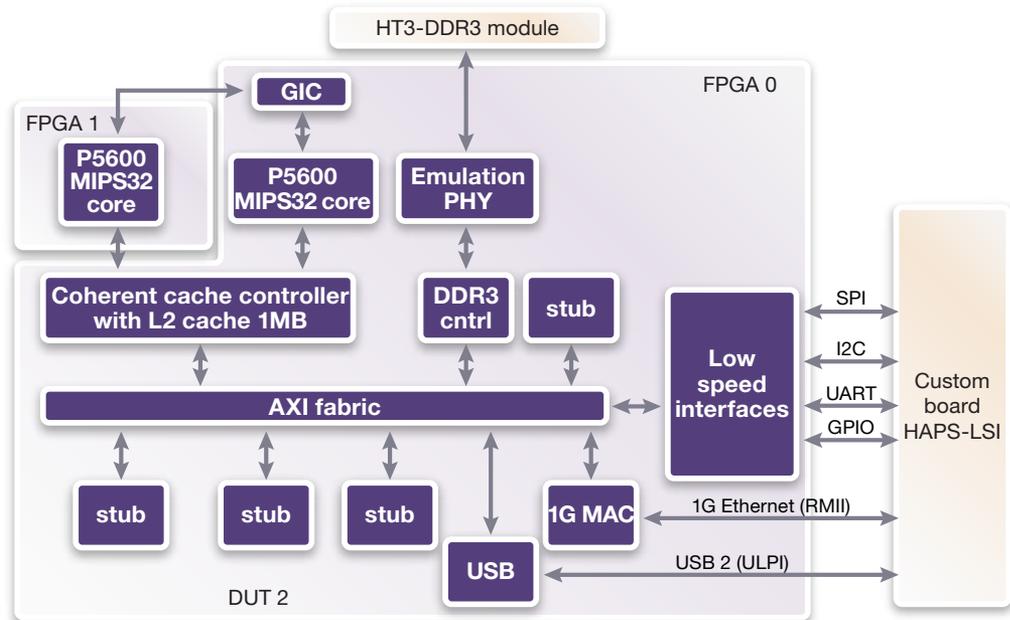


Figure 3: Stage Three Prototype - Baikal-T DUT2

Next, DUT2, a two-FPGA implementation, expanded the prototype design to incorporate both of the P5600 MIPS cores and replaced the simple SRAM memory with a DDR3 SDRAM.

The large number of clocks of the SoC required some careful planning in order to support the various peripheral interfaces. HAPS PLLs and dividers allowed the team to design several interface reference clocks and AXI and APB subsystem clocks as well as the inter-chip pin multiplexing and on-chip debugging.

Baikal developed verification subsystems for each major high-speed IO interface: SATA, PCI Express, and 10G Ethernet using a mix of Synopsys DesignWare IP and custom built interface boards for HapsTrak 3 and HapsTrak MGB.

An Improved HW/SW Validation Flow

Baikal's decision to use a mix of virtual and physical prototypes benefited the team by allowing them to start hardware/software integration tasks well before the entire RTL codebase was complete. Due to the project complexity and the need to start early hardware and software co-verification, Baikal Electronics decided to take a step-by-step incremental approach to prototyping the SoC, starting with a relatively simple to implement and debug system and then incrementally adding more components as soon as available.

The decision to start with a hybrid prototyping approach enabled the team to create a simple executable model of the system, uncover and debug functional errors early. The hybrid prototype allowed interaction tests between the CPU and other parts of the system when running real software code, and revealed a number of errors at the system level that ultimately improved the quality of the RTL design.