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# Synopsys and Allwinner Technology

## Allwinner Technology Selects Synopsys HAPS FPGA-Based Prototyping System for Their Largest Application Processor SoC Design

*"Synopsys' reputation as an established provider of FPGA-based prototyping solutions was a key factor in our decision to use HAPS for our A80 Octa SoC."*

**Ding Ran**
CTO, Allwinner Technology

Allwinner Technology, a leading fabless design house dedicated to the development of smart application processor system-on-chip (SoC) and smart analog integrated circuit (IC) technology, serves as a mainstream solution provider for tablet, mobile connected device and smart power management ICs in China.

### Challenges

- Design high-end application processor SoC featuring eight ARM big.LITTLE cores and a GPU core
- Hardware design validation of multi-CPU and GPU design

### Synopsys Solution

- HAPS® FPGA-Based Prototyping Systems

### Benefits

- High performance solution enabled greater validation depth in less time
- Excellent technical support and documentation

### Overview

Since its founding in 2007, Allwinner Technology has released multiple mobile application processors, largely implemented in Android-based smartphones, tablets, internet boxes and set-top boxes. Allwinner Technology needed a solution capable of high performance hardware and software validation for their A80 Octa architecture, an eight core SoC based on ARM's big.LITTLE processing technology. The A80 Octa SoC represents two heterogeneous ARM cores, consisting of quad core Cortex-A7 and Cortex-A15 processors in a big.LITTLE configuration, to deliver a design that optimizes high-performance and low-power in phones, tablets and other mobile devices. For increased performance resolution, the A80 design is also paired with a GPU core.


**Figure 1: Allwinner Technology A80 Octa System-On-Chip**

## HAPS Delivers High Performance

Allwinner's eight core-based SoC demanded a high performance validation solution to speed validation of their large SoC design. FPGA-based prototypes are the proven and essential methodology to perform large SoC validation tasks. Synopsys HAPS FPGA-based prototyping delivered the performance needed to validate Allwinner's A80 Octa SoC. The complexity of Allwinner's SoC increased both cost and schedule risks due to the need to verify real-world scenarios early in the development cycle. HAPS mitigated those challenges as a cost effective solution that achieved the performance required to validate Allwinner's SoC, while reducing ASIC design time and cutting months off their development schedule.

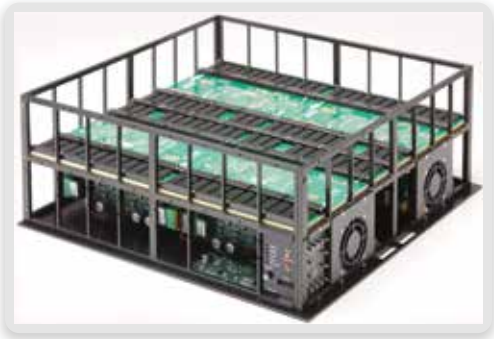

**Figure 2: HAPS-70 S48 FPGA-based Prototyping System**

## High-Quality Hardware and Support

Synopsys' premier reputation as a commercial provider of FPGA-based prototyping systems was instrumental in Allwinner's decision to select Synopsys HAPS hardware. The performance capabilities and completeness of the HAPS hardware, Certify prototyping software and technical documentation helped Allwinner efficiently verify that its SoC design met their specification. Selecting Synopsys HAPS allowed Allwinner to focus its engineering efforts on the validation of its SoC instead of the design of a custom validation platform, reducing the total engineering cost and project effort.

*"The performance capabilities of the HAPS system exceeded our needs and enabled our designers to perform accurate validation of our largest SoC. Synopsys is an outstanding supplier, living up to their excellent reputation of high-quality and high performance hardware."*

**Ding Ran**
CTO, Allwinner Technology



**Synopsys, Inc. • 700 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com**


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