

Synopsys and Teradici

ASIC Prototyping Made Fast and Efficient with Synplify Premier



Other tools can't handle the complex constructs of the ASICs we're working on. Only Synplify Premier gives us the ability to synthesize native ASIC code untouched for our FPGA prototype."



David Garau

Engineering Manager, Silicon Validation Group, Teradici

Business

Teradici drives innovation to fundamentally change the way people use and deploy computers by developing technology and solutions that deliver a true, uncompromised PC user experience over IP networks.

Challenges

- ▶ Need faster turnaround timing while meeting timing closure goals
- ▶ Retarget native ASIC code and synthesize for FPGA-based prototype
- ▶ Track bugs back to the root cause

System-Level Design Solution

- ▶ Synplify® Premier Advanced FPGA Design Tool
- ▶ Identify® RTL Debug Tool
- ▶ DesignWare® IP

Benefits

- ▶ Achieve high timing QoR by optimizing inside Xilinx core IP for fewer design iterations
- ▶ Seamlessly retarget ASIC code to FPGA-based prototype, with RTL compatibility, DesignWare support in FPGAs, and gated clock conversion
- ▶ Gain high visibility in debugging with "qualified sampling" capability

Overview

Teradici focuses on designing advanced image processing algorithms enabling the physical separation of the computer and the user, changing enterprise computing. Their unique display protocol called PC-over-IP® or PCoIP® Technology.

The TERA Host and zero client chipset enables centralized computing to span a standard enterprise network from the datacenter to the desktop. The TERA chipset implements advanced display compression algorithms and I/O bridging to guarantee a high performance, uncompromised user experience. The TERA chipset includes the TERA1100 PCoIP zero client processor and TERA1200 PCoIP host processor, the first in a family of PCoIP technology based devices.

For previous generations of Teradici products, the Silicon Validation Group relied on Synplify Pro® Logic Synthesis and Identify® RTL Debugger to retarget their ASIC design into an FPGA-based prototype. As Xilinx chips became more advanced and timing closure goals harder to achieve, the team moved to Synplify Premier FPGA design tool with its more advanced timing optimization technology, Identify RTL debugger, and DesignWare integration built in.



Identify is invaluable because of the great visibility it provides into bugs that we can trace back to either hardware or software, quickly identifying the source without data buffer overload.”

David Garau

Engineering Manager, Silicon Validation Group, Teradici

Leading FPGA Design Solution

The Silicon Validation Group’s most current project involves nine FPGAs in a single platform with various DesignWare IP such as PCIe and USB. The design includes both Xilinx Virtex®-5 220 and Xilinx Virtex-5 330 devices. Both imaging and PC components are a part of the design.

Because Teradici needs to prototype complex ASIC constructs, they need an advanced FPGA synthesis and debug tool. The Synplify Premier software gives the Silicon Validation Group more control and faster synthesis by reading in Xilinx IP cores (e.g., RAM blocks) as part of the timing flow. Synplify Premier is able to deliver high QoR with the “Enhanced Logic Synthesis” mode which optimizes the logic inside Xilinx core IP. Synplify Premier provided such good timing QoR that this allowed them to turn off optimizations in the Xilinx backend P&R tool, saving significant P&R runtime.

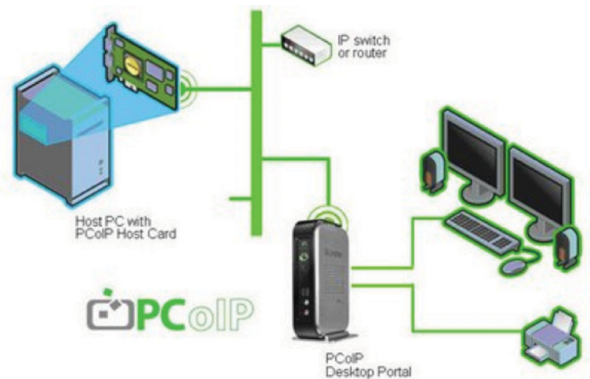
For the timing critical FPGAs, turnaround time (TAT) from RTL to bitfile was reduced from 11-13 hours to 7-8 hours. Synplify Premier software also enables the team to specify multiple clock domains in about 60% of these FPGA devices.

The Silicon Validation Group also needs an FPGA synthesis tool that can retarget their ASIC code into a prototype. Not only can Synplify Premier seamlessly retarget their native ASIC code, but it can also easily synthesize the DesignWare ASIC cores that they are using in the design. David Garau said,

“Synplify Premier’s gated clock conversion capability is a must have. It works so well we don’t even have to think about it.”

Another important component of Synplify Premier’s capabilities for this design project is the integrated Identify debug tool. Between a team of both hardware and software engineers, tracking bugs back to the root cause is often time consuming and difficult. With the Identify RTL debugger’s “qualified sampling” capability the Teradici design team is able to very selectively collect specific data from instrumented signals, allowing them to extract valuable information over an extended period without data buffer overload. The design team finds the user interface very intuitive.

With Synplify Premier, the Teradici Silicon Validation Group has a proven flow to prototype their next generation ASIC design.



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Engineering Manager, Silicon Validation Group, Teradici



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