

Timing Constraints Manager

**Best-in-class,
no-noise SDC
verification,
generation and
management
solution**

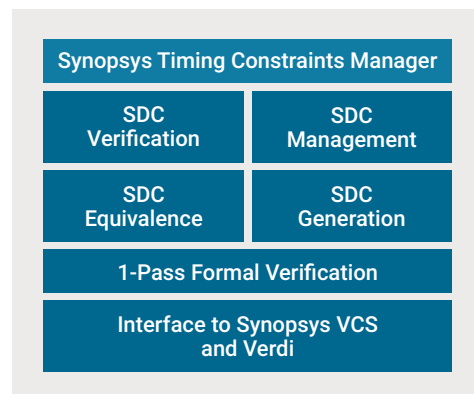
Overview

Synopsys Timing Constraints Manager improves chip design process by automatically generating, managing, and verifying timing constraints early in the design cycle. Synopsys Timing Constraints Manager can be seamlessly integrated with Synopsys Digital Design and Verification families with consistent constraint support for single-pass constraints closure to address and improve designer productivity significantly.

Synopsys Timing Constraints Manager helps designers by:

- Providing precise feedback on their SDC bugs
- Providing tape-out proven promotion, demotion, and mapping solutions
- Reducing designer SDC review effort and improving development schedule

Synopsys Timing Constraints Manager offers a unique approach where-in the tool employs correct-by-construction, 1-pass formal verification to root-cause real constraints bugs and prevent silicon failure with no noise.



SDC Verification

SDC verification flow using Synopsys Timing Constraints Manager reads the RTL description for a design along with either gate or RTL level Tcl constraints. The tool further maps the constraints to the design, flagging syntax and constraint application issues. The constraints are formally proven and issues are presented to the user for review using a powerful debug environment. Constraints that fail formal proof are converted into assertions for use during RTL simulation.

SDC Management

SDC management using Synopsys Timing Constraints Manager takes SDC or Tcl constraints from one design representation and transforms it to another, working with either RTL or netlist input. The tool is used to map RTL constraints to the gate-level, transform gate-level constraints to make them applicable at RTL, promote IP constraints into an SoC, demote SoC constraints down to implementation blocks, and merge multi-mode constraints into a single super-mode. The integrity of all these transformations is verified using an SDC equivalence verification solution.

SDC Generation

SDC generation using Synopsys Timing Constraints Manager reads the RTL for a design, and from just that information generates the clock definitions, input-output delays, clock groups, clock senses and timing exceptions for the design. As an option, the tool can also be asked to identify the modes on the design and the case analyses that put the design into a specific mode. Users can also generate .lib models from RTL and these models can then be used for design budgeting while the implementation of a block is still in progress. The constraints generated by the tool are verified using an SDC verification solution.

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